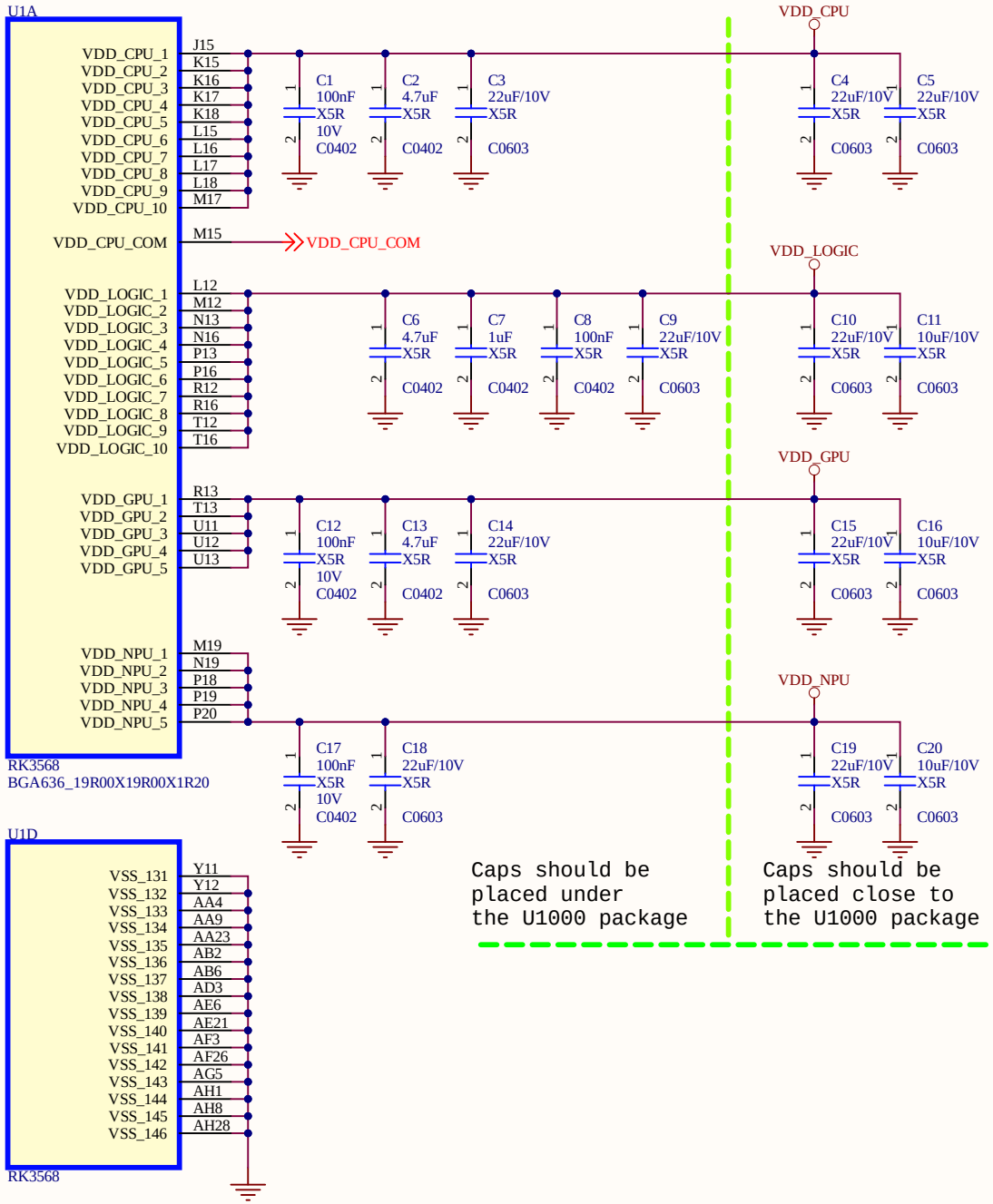
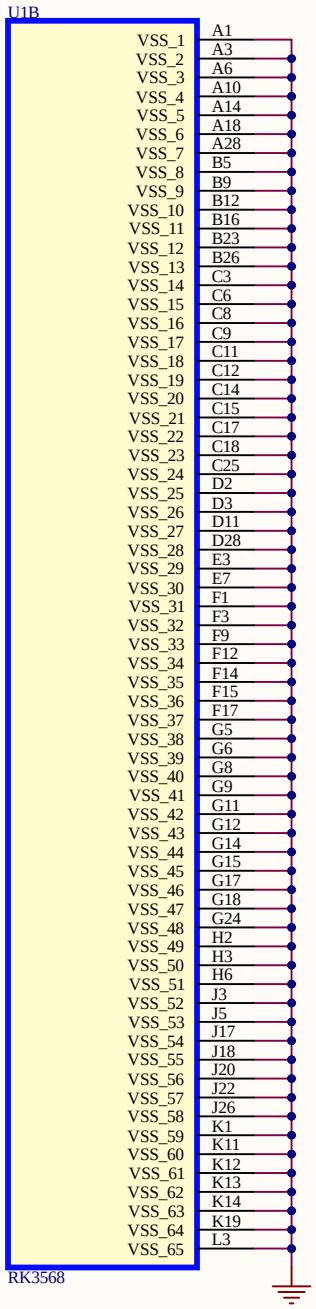
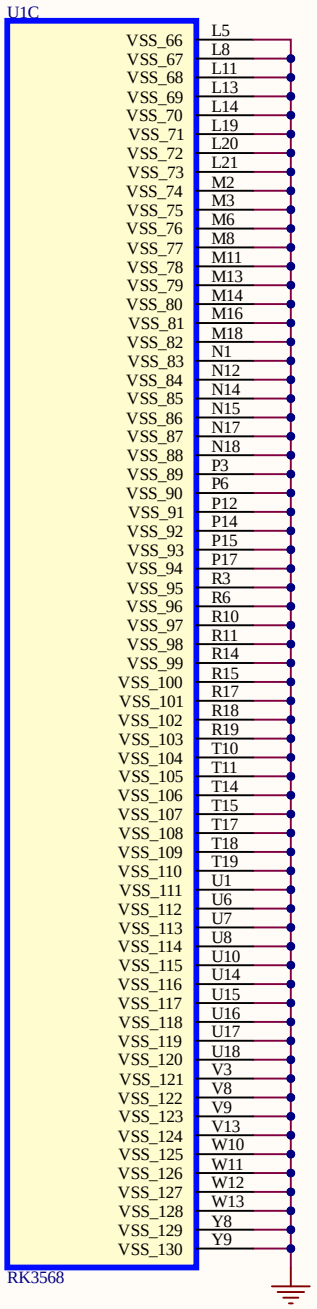
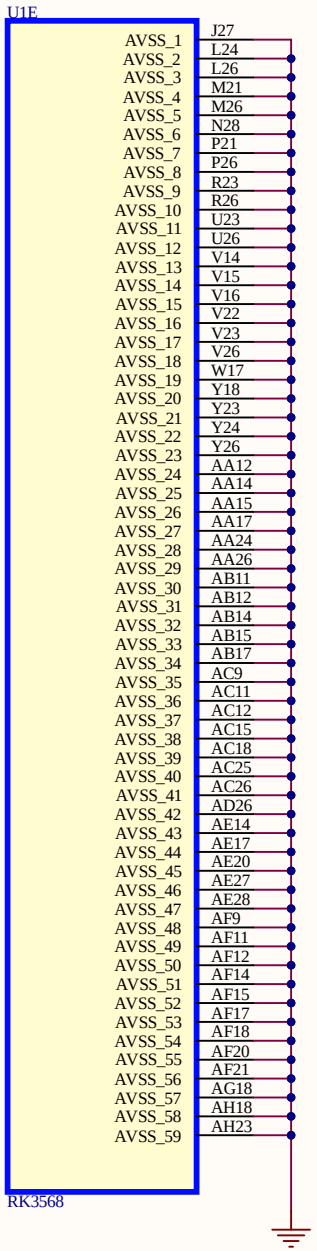
RK3568_ABCDE (Power&Gnd)

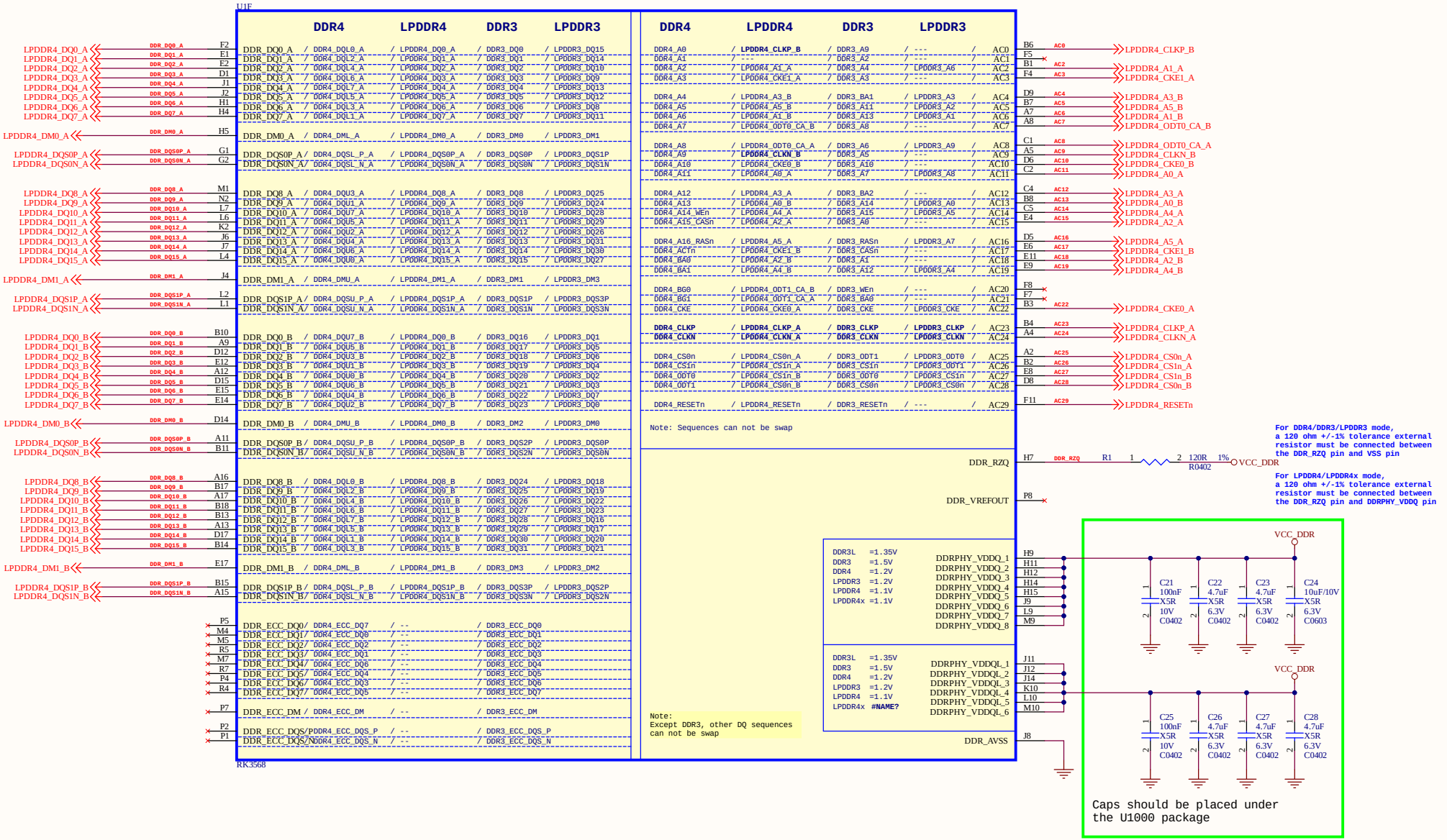






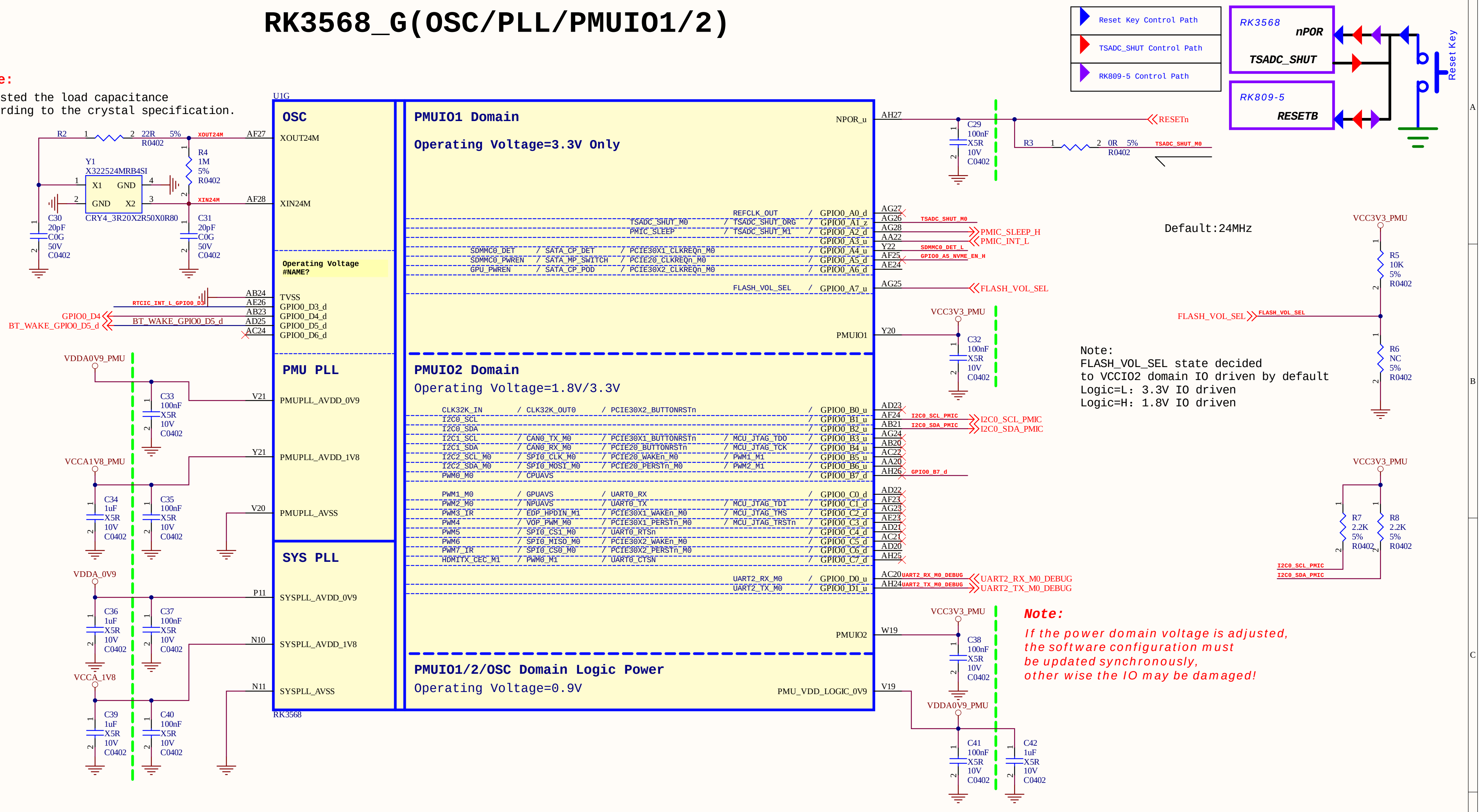


RK3568_F (DDR PHY)



RK3568_G(OSC/PLL/PMUIO1/2)

Note:
Adjusted the load capacitance
according to the crystal specification.

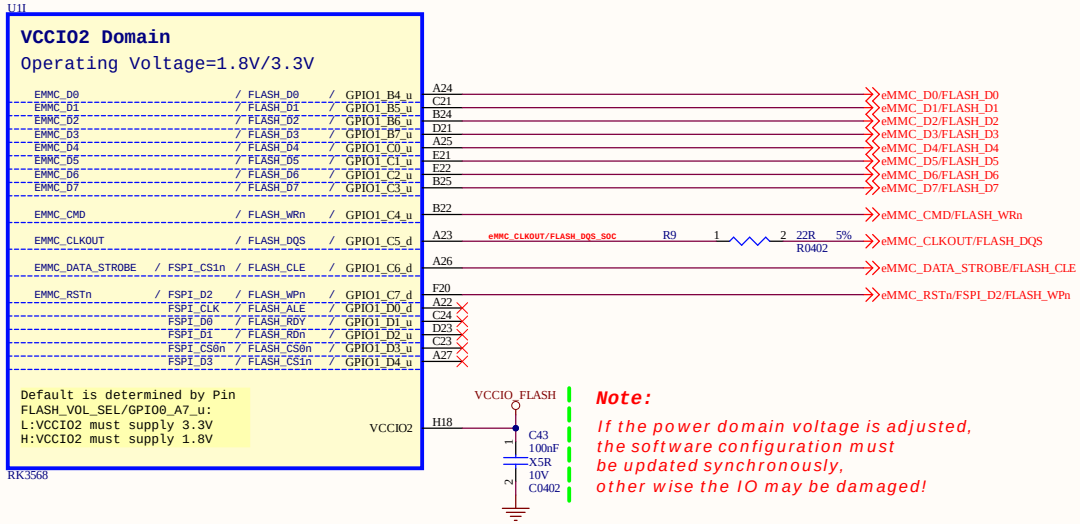


Note:
FLASH_VOL_SEL state decided
to VCCIO2 domain IO driven by default
Logic=L: 3.3V IO driven
Logic=H: 1.8V IO driven

Note:
If the power domain voltage is adjusted,
the software configuration must
be updated synchronously,
other wise the IO may be damaged!

Note:
Caps of between dashed green lines and U1000
should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

RK3568_I(VCCIO2 Domain)



Note:

If the power domain voltage is adjusted,
the software configuration must
be updated synchronously,
other wise the IO may be damaged!

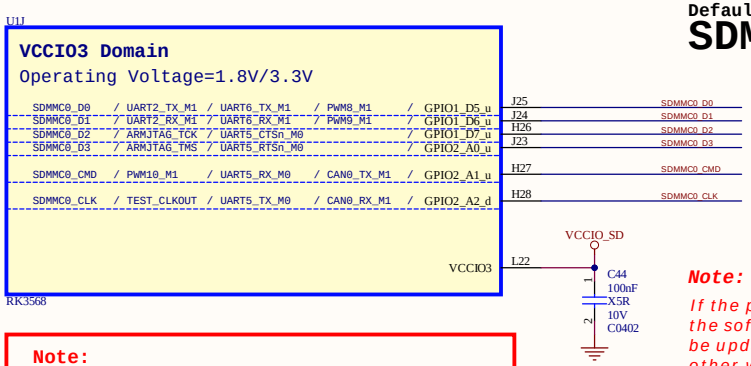
Layout note:

Test point must be placed on the line, and no branch can be added

Note:
Reserve TestPoint for put the system into Maskrom mode to update the firmware
When writing mismatched firmware or other conditions result in boot failure,
use this test point

Except in this case, please use Recovery Key
Put the system into loader mode to update the firmware

RK3568_J(VCCIO3 Domain)



Default
SDMMC0&JTAG

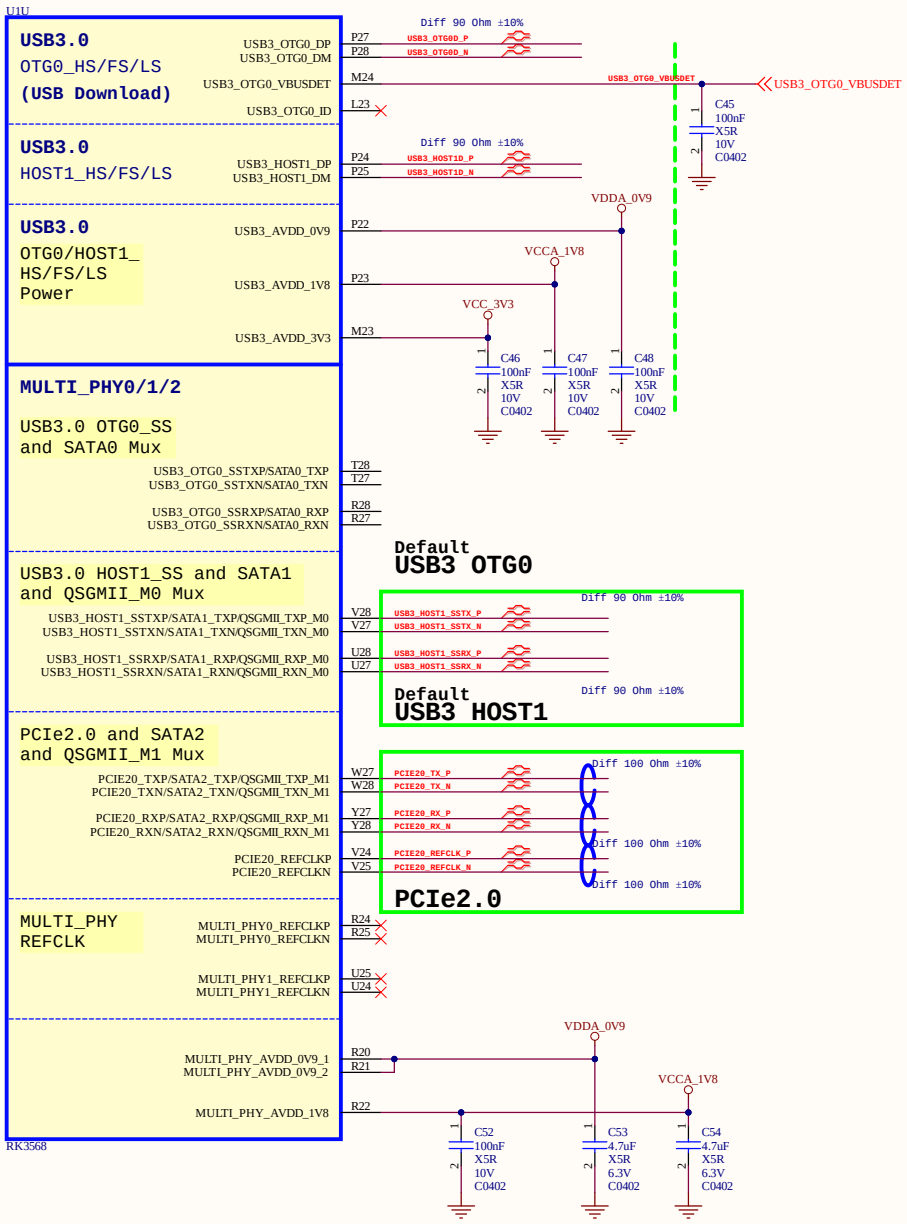
Note:

If the power domain voltage is adjusted,
the software configuration must
be updated synchronously,
other wise the IO may be damaged!

Note:

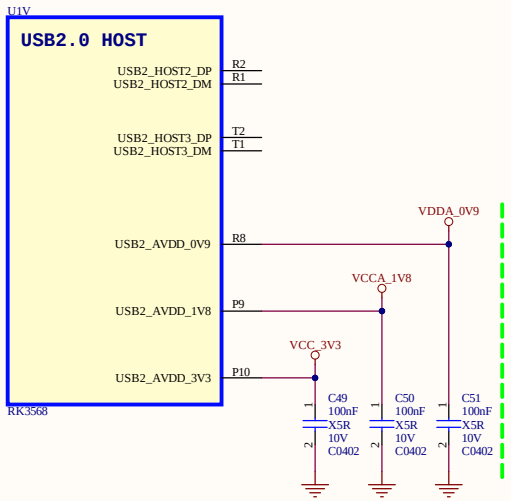
Caps of between dashed green lines and U1000
should be placed under the U1000 package

RK3568_U(USB3.0/SATA/QSGMII/PCIe2.0 x1)

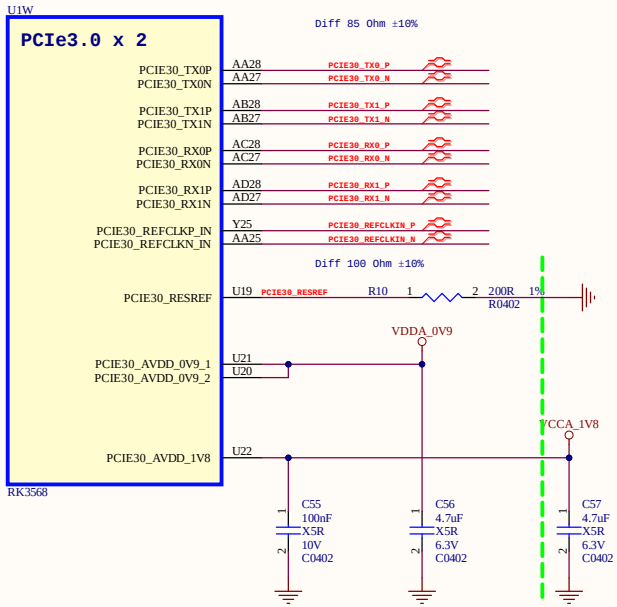


Note:
Caps of between dashed green lines and U1000
should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

RK3568_V(USB2.0 HOST)



RK3568_W(PCIe3.0 x2)



RK3568_K(VCCIO4 Domain)

U1K

VCCIO4 Domain

Operating Voltage=1.8V/3.3V

SDMMC1_D0	GMAC0_RXD2	UART6_RX_M0		GPIO2_A3_u	E27 GMAC0_RXD2 → GMAC0_RXD2
SDMMC1_D1	GMAC0_RXD3	UART6_TX_M0		GPIO2_A4_u	E28 GMAC0_RXD3 → GMAC0_RXD3
SDMMC1_D2	GMAC0_RXCLK	UART7_RX_M0		GPIO2_A5_u	B28 GMAC0_RXCLK → GMAC0_RXCLK
SDMMC1_D3	GMAC0_TXD2	UART7_TX_M0		GPIO2_A6_u	C27 GMAC0_TXD2 → GMAC0_TXD2
SDMMC1_CMD	GMAC0_TXD3	UART9_RX_M0		GPIO2_A7_u	C28 GMAC0_TXD3 → GMAC0_TXD3
SDMMC1_CLK	GMAC0_TXCLK	UART9_TX_M0		GPIO2_B0_d	D27 GMAC0_TXCLK → GMAC0_TXCLK
SDMMC1_PWREN	I2C4_SDA_M1	UART8_RTSn_M0	CAN2_RX_M1	GPIO2_B1_d	D26 → UART8_RTSn_M0
SDMMC1_DET	I2C4_SCL_M1	UART8_CTSn_M0	CAN2_TX_M1	GPIO2_B2_u	E25 → UART8_CTSn_M0
	GMAC0_TXD0	UART1_RX_M0		GPIO2_B3_u	F28 GMAC0_TXD0 → GMAC0_TXD0
	GMAC0_TXD1	UART1_TX_M0		GPIO2_B4_u	G27 GMAC0_TXD1 → GMAC0_TXD1
	GMAC0_TXEN	UART1_RTSn_M0	SPI1_CLK_M0	GPIO2_B5_u	G28 GMAC0_TXEN → GMAC0_TXEN
	GMAC0_RXD0	UART1_CTSn_M0	SPI1_MISO_M0	GPIO2_B6_u	F27 GMAC0_RXD0 → GMAC0_RXD0
I2S2_SCLK_RX_M0	GMAC0_RXD1	UART6_RTSn_M0	SPI1_MOSI_M0	GPIO2_B7_d	H25 GMAC0_RXD1 → GMAC0_RXD1
I2S2_LRCK_RX_M0	GMAC0_RXDV_CRS	UART6_CTSn_M0	SPI1_CS0_M0	GPIO2_C0_d	F24 GMAC0_RXDV_CRS → GMAC0_RXDV_CRS
I2S2_MCLK_M0	ETH0_REFCLKO_25M	UART7_RTSn_M0	SPI2_CLK_M0	GPIO2_C1_d	G23
I2S2_SCLK_TX_M0	GMAC0_MCLKINOUT	UART7_CTSn_M0	SPI2_MISO_M0	GPIO2_C2_d	F25 GMAC0_MCLKINOUT → GMAC0_MCLKINOUT
I2S2_LRCK_TX_M0	GMAC0_MDC	UART9_RTSn_M0	SPI2_MOSI_M0	GPIO2_C3_d	H24 GMAC0_MDC → GMAC0_MDC
I2S2_SDO_M0	GMAC0_MDIO	UART9_CTSn_M0	SPI2_CS0_M0	GPIO2_C4_d	H23 GMAC0_MDIO → GMAC0_MDIO
I2S2_SDI_M0	GMAC0_RXER	UART8_TX_M0	SPI2_CS1_M0	GPIO2_C5_d	F26 → UART8_TX_M0
CLK32K_OUT1		UART8_RX_M0	SPI1_CS1_M0	GPIO2_C6_d	E26 → UART8_RX_M0

VCCIO4

RK3568

VCCIO4 — J21 — C58 100nF X5R 10V C0402

Note:

If the power domain voltage is adjusted, the software configuration must be updated synchronously, other wise the IO may be damaged!

VCCIO4 — R11 1 2 0R 5% R0402 — VCC_1V8

VCCIO4 — R12 1 2 NC 5% R0402 — VCC_3V3

RGMII0+UART8

Note:

If Ethernet PHY uses other models, please note whether the default pull-up and pull-down of GPIO affect Ethernet PHY function

At present, TXEN will be affected if it defaults to high level need to add a 4.7K resistance to ground

If Ethernet PHY uses other models, please note whether the default pull-up and pull-down of GPIO affect Ethernet PHY function

At present, TXEN will be affected if it defaults to high level need to add a 4.7K resistance to ground

Note:

According to the actual choice of mounted Cannot be mounted at the same time

Default:1.8V

Select the voltage according to the application

RK3568_N(VCCIO7 Domain)

U1N

VCCIO7 Domain

Operating Voltage=1.8V/3.3V

PWM14_M1	SPI3_CLK_M1	CAN1_RX_M1	PCIE30X2_CLKREQn_M2	GPIO4_C2_d	AF8 GPIO4_C2
PWM15_IR_M1	SPI3_MOSI_M1	CAN1_TX_M1	PCIE30X2_WAKEn_M2	GPIO4_C3_d	AA11
EDP_HPDIN_M0	SPDIF_TX_M2	SATA2_ACT_LED	PCIE30X2_PERSTn_M2	GPIO4_C4_d	AH7 BT_RST_GPIO4_C4 → BT_RST_GPIO4_C4
PWM12_M1	SPI3_MISO_M1	SATA1_ACT_LED	UART9_TX_M1	GPIO4_C5_d	AD8
PWM13_M1	SPI3_CS0_M1	SATA0_ACT_LED	UART9_RX_M1	GPIO4_C6_d	AE8
HDMITX_SCL	I2C5_SCL_M1			GPIO4_C7_u	AG8 → HDMITX_SCL
HDMITX_SDA	I2C5_SDA_M1			GPIO4_D0_u	AG7 → HDMITX_SDA
HDMITX_CEC_M0	SPI3_CS1_M1			GPIO4_D1_u	AH6 → HDMITX_CEC_M0
				GPIO4_D2_d	AB9

VCCIO7 — V12 — VCC_3V3 — C61 100nF X5R 10V C0402

RK3568

Note:

If the power domain voltage is adjusted, the software configuration must be updated synchronously, other wise the IO may be damaged!

Default

GPIO4_C5 → UART9_TX_M1

GPIO4_C6 → UART9_RX_M1

Option

GPIO4_C5 → SATA1_ACT_LED

GPIO4_C6 → SATA0_ACT_LED

RK3568_O(SARADC/OTP)

U1O

SARADC

Recovery	SARADC_VIN0	B27	SARADC_VIN0_KEY/RECOVERY — C59 1 2 1nF X5R 50V C0402
	SARADC_VIN1	C26	SARADC_VIN1_HW_ID — C60 1 2 1nF X5R 50V C0402
	SARADC_VIN2	D24	
	SARADC_VIN3	E23	
	SARADC_VIN4	G21	
	SARADC_VIN5	F22	
	SARADC_VIN6	G20	
	SARADC_VIN7	F21	
	SARADC_AVDD_1V8	H22	VCCA_1V8 — C62 100nF X5R 10V C0402

OTP

OTP_VCC18 — H20 — VCC_1V8 — C63 100nF X5R 10V C0402

VCCA_1V8 — R14 10K 1% R0402 — SARADC_VIN1_HW_ID — R15 10K 1% R0402

RK3568

Note:

Caps of between dashed green lines and U1000 should be placed under the U1000 package

Note:

Must be mounted

VCCA_1V8 — R13 10K 1% R0402 — SARADC_VIN0_KEY/RECOVERY — GND

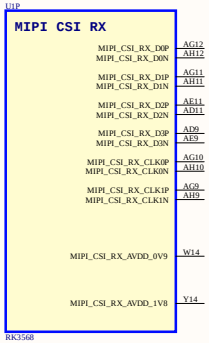
Note:

If there is no Key requirement, two test points must be reserved to facilitate firmware update

It is suggested to reserve a Key to facilitate the development debug

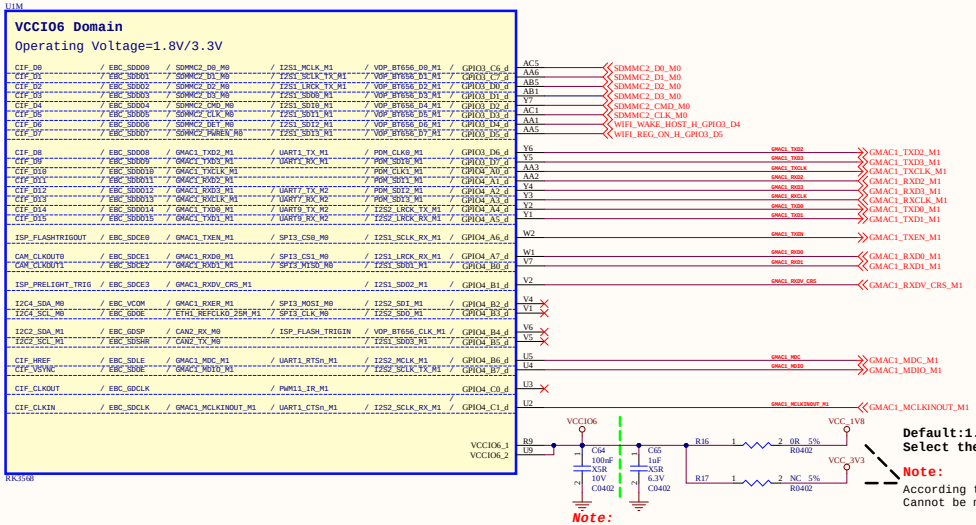
If SARADC_VIN0=0V at after power on and reset, then system will enter into loader mode.

RK3568_P(MIPI_CSI_RX)



Option1	Sensor1 x4Lane	MIPI_CSI_RX_D0-3 MIPI_CSI_RX_CLK0
Option2	Sensor1 x2Lane + Sensor2 x2Lane	MIPI_CSI_RX_D0-1 MIPI_CSI_RX_CLK0 MIPI_CSI_RX_D2-3 MIPI_CSI_RX_CLK1

RK3568_M(VCCIO6 Domain)



Default:1.8V
Select the voltage according to the application

Note:
According to the actual choice of mounted
Cannot be mounted at the same time

Note:
If the power domain voltage is adjusted,
the software configuration must
be updated synchronously,
other wise the IO may be damaged!

Note:
Caps of between dashed green lines and U1000
should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

Note:
Camera MCLK can select the following clock:
1:CAM_CLKOUT0
2:CAM_CLKOUT1
3:CIF_CLKOUT
4:REFCLK_OUT

Attention to the voltage matching

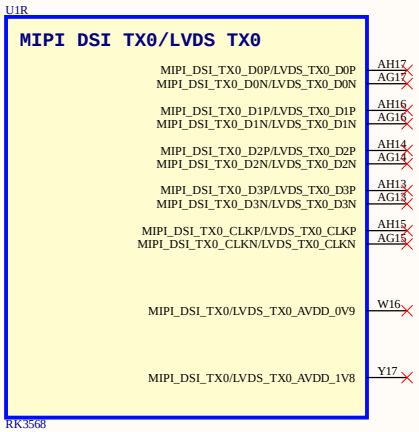
Mode	16bit	12bit	10bit	8bit
CIF_D0	D0	--	--	--
CIF_D1	D1	--	--	--
CIF_D2	D2	--	--	--
CIF_D3	D3	--	--	--
CIF_D4	D4	D0	--	--
CIF_D5	D5	D1	--	--
CIF_D6	D6	D2	D0	--
CIF_D7	D7	D3	D1	--
CIF_D8	D8	D4	D2	D0
CIF_D9	D9	D5	D3	D1
CIF_D10	D10	D6	D4	D2
CIF_D11	D11	D7	D5	D3
CIF_D12	D12	D8	D6	D4
CIF_D13	D13	D9	D7	D5
CIF_D14	D14	D10	D8	D6
CIF_D15	D15	D11	D9	D7

Support BT601 YCbCr 422 8bit input
Support BT656 YCbCr 422 8bit input
Support RAW 8/10/12bit input
Support BT1120 YCbCr 422 8/10/12/16bit input, single/dual-edge sampling
Support 2/4 mixed BT656/BT1120 YCbCr 422 8bit input

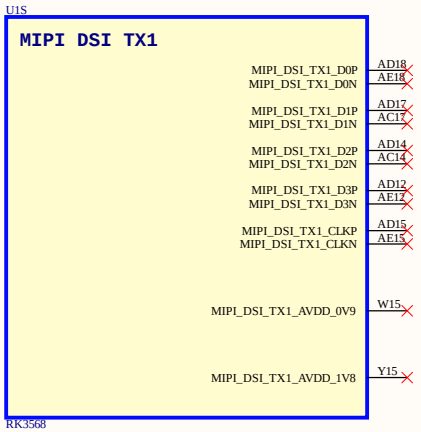
BT1120 16bit Mode:
Default: D0-D7 <--> Y0-Y7 , D8-D15 <--> C0-C7
Swap ON: D0-D7 <--> C0-C7 , D8-D15 <--> Y0-Y7

GMAC	Direction	GEPHY	GMAC	Direction	FEPHY
GMACx_TXD0	------->	PHYx_TXD0	GMACx_TXD0	------->	PHYx_TXD0
GMACx_TXD1	------->	PHYx_TXD1	GMACx_TXD1	------->	PHYx_TXD1
GMACx_TXD2	------->	PHYx_TXD2			
GMACx_TXD3	------->	PHYx_TXD3			
GMACx_TXEN	------->	PHYx_TXEN	GMACx_TXEN	------->	PHYx_TXEN
GMACx_TXCLK	------->	PHYx_TXCLK			
GMACx_RXD0	<-------	PHYx_RXD0	GMACx_RXD0	<-------	PHYx_RXD0
GMACx_RXD1	<-------	PHYx_RXD1	GMACx_RXD1	<-------	PHYx_RXD1
GMACx_RXD2	<-------	PHYx_RXD2			
GMACx_RXD3	<-------	PHYx_RXD3			
GMACx_RXDV	<-------	PHYx_RXDV	GMACx_RXDV	<-------	PHYx_RXDV
GMACx_RXCLK	<-------	PHYx_RXCLK			
GMACx_RXER			GMACx_RXER	<-------	PHYx_RXER
GMACx_MDC	------->	PHYx_MDC	GMACx_MDC	------->	PHYx_MDC
GMACx_MDIO	<------>	PHYx_MDIO	GMACx_MDIO	<------>	PHYx_MDIO
ETHx_REFCLKO_25M	------->	PHYx_XTALIN			
GMACx_MCLKINOUT	<-------	PHYx_CLKOUT125(Option)	GMACx_MCLKINOUT	------->	PHYx_XTALIN/REFCLK
GPIO	------->	PHYx_RSTn	GPIO	------->	PHYx_RSTn
GPIO	<-------	PHYx_INT/PMEB	GPIO	<-------	PHYx_INT/PMEB

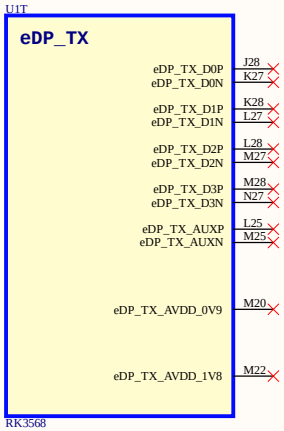
RK3568_R(MIPI_DSI_TX0/LVDS_TX0)



RK3568_S(MIPI_DSI_TX1)

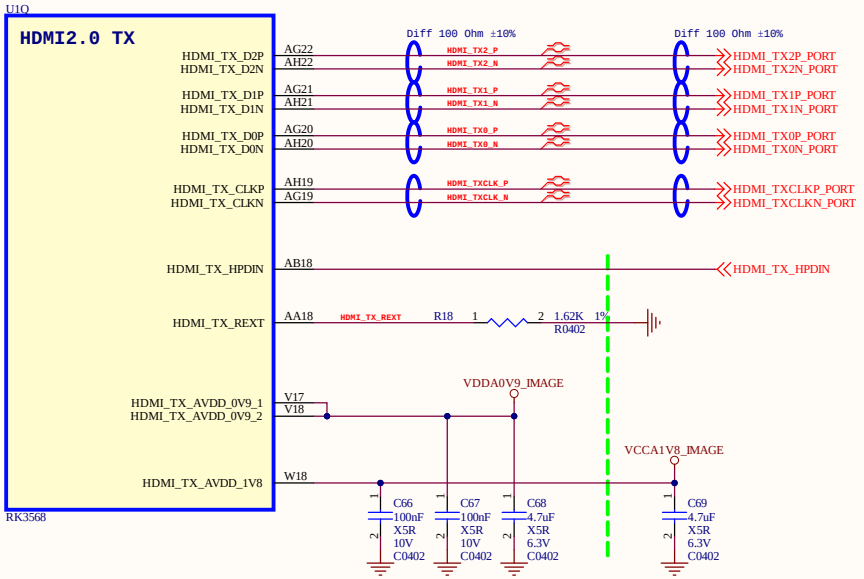


RK3568_T(eDP TX)



Note:
Caps of between dashed green lines and U1000
should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

RK3568_Q(HDMI2.0 TX)



RK3568_L(VCCIO5 Domain)

U1L

VCCIO5 Domain

Operating Voltage=1.8V/3.3V

LCDC_D0	VOP_BT656_D0_M0	SPI0_MISO_M1	PCIE20_CLKREQn_M1	I2S1_MCLK_M2	GPIO2_D0_d	AG6
LCDC_D1	VOP_BT656_D1_M0	SPI0_MOSI_M1	PCIE20_WAKEn_M1	I2S1_SCLK_TX_M2	GPIO2_D1_d	AD7
LCDC_D2	VOP_BT656_D2_M0	SPI0_CS0_M1	PCIE30X1_CLKREQn_M1	I2S1_LRCK_TX_M2	GPIO2_D2_d	AC8
LCDC_D3	VOP_BT656_D3_M0	SPI0_CLK_M1	PCIE30X1_WAKEn_M1	I2S1_SDI0_M2	GPIO2_D3_d	AC7
LCDC_D4	VOP_BT656_D4_M0	SPI2_CS1_M1	PCIE30X2_CLKREQn_M1	I2S1_SDI1_M2	GPIO2_D4_d	AF5
LCDC_D5	VOP_BT656_D5_M0	SPI2_CS0_M1	PCIE30X2_WAKEn_M1	I2S1_SDI2_M2	GPIO2_D5_d	AF6
LCDC_D6	VOP_BT656_D6_M0	SPI2_MOSI_M1	PCIE30X2_PERSTn_M1	I2S1_SDI3_M2	GPIO2_D6_d	AD6
LCDC_D7	VOP_BT656_D7_M0	SPI2_MISO_M1	UART8_TX_M1	I2S1_SDO0_M2	GPIO2_D7_d	AH5
LCDC_CLK	VOP_BT656_CLK_M0	SPI2_CLK_M1	UART8_RX_M1	I2S1_SDO1_M2	GPIO3_A0_d	AH4
LCDC_D8	VOP_BT1120_D0	SPI1_CS0_M1	PCIE30X1_PERSTn_M1	SDMMC2_D0_M1	GPIO3_A1_d	AB8
LCDC_D9	VOP_BT1120_D1	GMAC1_TXD2_M0	I2S3_MCLK_M0	SDMMC2_D1_M1	GPIO3_A2_d	AE5
LCDC_D10	VOP_BT1120_D2	GMAC1_TXD3_M0	I2S3_SCLK_M0	SDMMC2_D2_M1	GPIO3_A3_d	AG4
LCDC_D11	VOP_BT1120_D3	GMAC1_RXD2_M0	I2S3_LRCK_M0	SDMMC2_D3_M1	GPIO3_A4_d	AF4
LCDC_D12	VOP_BT1120_D4	GMAC1_RXD3_M0	I2S3_SDO_M0	SDMMC2_CMD_M1	GPIO3_A5_d	AH3
LCDC_D13	VOP_BT1120_CLK	GMAC1_TXCLK_M0	I2S3_SDI_M0	SDMMC2_CLK_M1	GPIO3_A6_d	AG3
LCDC_D14	VOP_BT1120_D5	GMAC1_RXCLK_M0		SDMMC2_DET_M1	GPIO3_A7_d	AH2
LCDC_D15	VOP_BT1120_D6	ETH1_REFCLKO_25M_M0		SDMMC2_PWREN_M1	GPIO3_B0_d	AG2
LCDC_D16	VOP_BT1120_D7	GMAC1_RXD0_M0	UART4_RX_M1	PWM8_M0	GPIO3_B1_d	AG1
LCDC_D17	VOP_BT1120_D8	GMAC1_RXD1_M0	UART4_TX_M1	PWM9_M0	GPIO3_B2_d	AF2
LCDC_D18	VOP_BT1120_D9	GMAC1_RXDV_CRS_M0	I2C5_SCL_M0	PDM_SDI0_M2	GPIO3_B3_d	AF1
LCDC_D19	VOP_BT1120_D10	GMAC1_RXER_M0	I2C5_SDA_M0	PDM_SDI1_M2	GPIO3_B4_d	AE1
LCDC_D20	VOP_BT1120_D11	GMAC1_TXD0_M0	I2C3_SCL_M1	PWM10_M0	GPIO3_B5_d	AE2
LCDC_D21	VOP_BT1120_D12	GMAC1_TXD1_M0	I2C3_SDA_M1	PWM11_IR_M0	GPIO3_B6_d	AE3
LCDC_D22	PWM12_M0	GMAC1_TXEN_M0	UART3_TX_M1	PDM_SDI2_M2	GPIO3_B7_d	AD4
LCDC_D23	PWM13_M0	GMAC1_MCLKINOUT_M0	UART3_RX_M1	PDM_SDI3_M2	GPIO3_C0_d	AD2
LCDC_HSYNC	VOP_BT1120_D13	SPI1_MOSI_M1	PCIE20_PERSTn_M1	I2S1_SDO2_M2	GPIO3_C1_d	AD1
LCDC_VSYNC	VOP_BT1120_D14	SPI1_MISO_M1	UART5_TX_M1	I2S1_SDO3_M2	GPIO3_C2_d	AA7
LCDC_DEN	VOP_BT1120_D15	SPI1_CLK_M1	UART5_RX_M1	I2S1_SCLK_RX_M2	GPIO3_C3_d	AC4
PWM14_M0	VOP_PWM_M1	GMAC1_MDC_M0	UART7_TX_M1	PDM_CLK1_M2	GPIO3_C4_d	AC3
PWM15_IR_M0	SPDIF_TX_M1	GMAC1_MDIO_M0	UART7_RX_M1	I2S1_LRCK_RX_M2	GPIO3_C5_d	AC2
					VCCIO5_1	V10
					VCCIO5_2	V11

RK3568

AG6 GMAC1_INT/PMEB_GPIO2_D0
AD7 GMAC1_RSTN_GPIO2_D1
AC8 GMAC0_INT/PMEB_GPIO2_D2
AC7 GMAC0_RSTN_GPIO2_D3
AF5 PCIE30X2_CLKREQn_M1
AF6 PCIE30X2_WAKEn_M1
AD6 PCIE30X2_PERSTn_M1
AH5 GPIO2_D7
AG4 LAN3_PERSTn_GPIO3_A3
AF4 LAN4_PERSTn_GPIO3_A4
AH3 GPIO3_A5
AG1 PWR_25G_GPIO3_B1
AF1 I2C5_SCL_M0
AE1 I2C5_SDA_M0
AD1 PCIE20_PERSTn_M1_GPIO3_C1
AA7 UART5_TX_M1
AC4 UART5_RX_M1
AC3 UART7_TX_M1
AC2 UART7_RX_M1

VCC_3V3

R19 NC 5% R0402
R20 NC 5% R0402
R900,R901为2.2K不贴

VCC_3V3

C70 100nF X5R 10V C0402

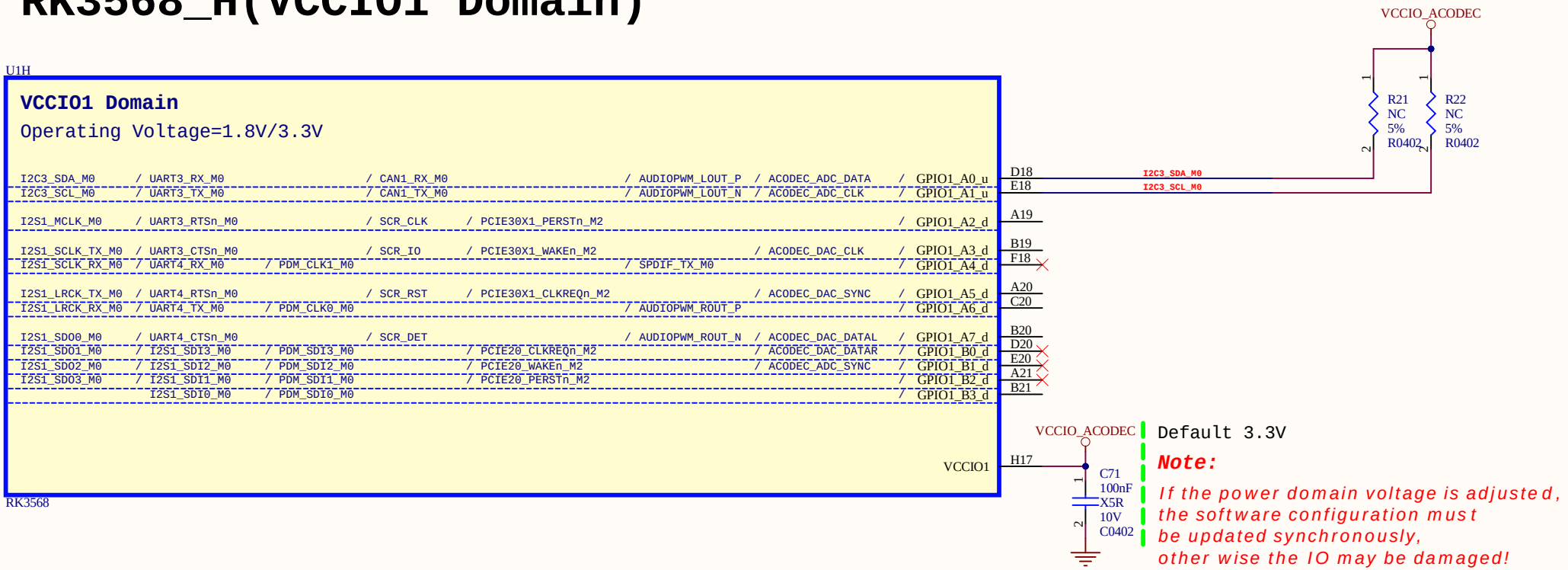
Note:

If the power domain voltage is adjusted, the software configuration must be updated synchronously, other wise the IO may be damaged!

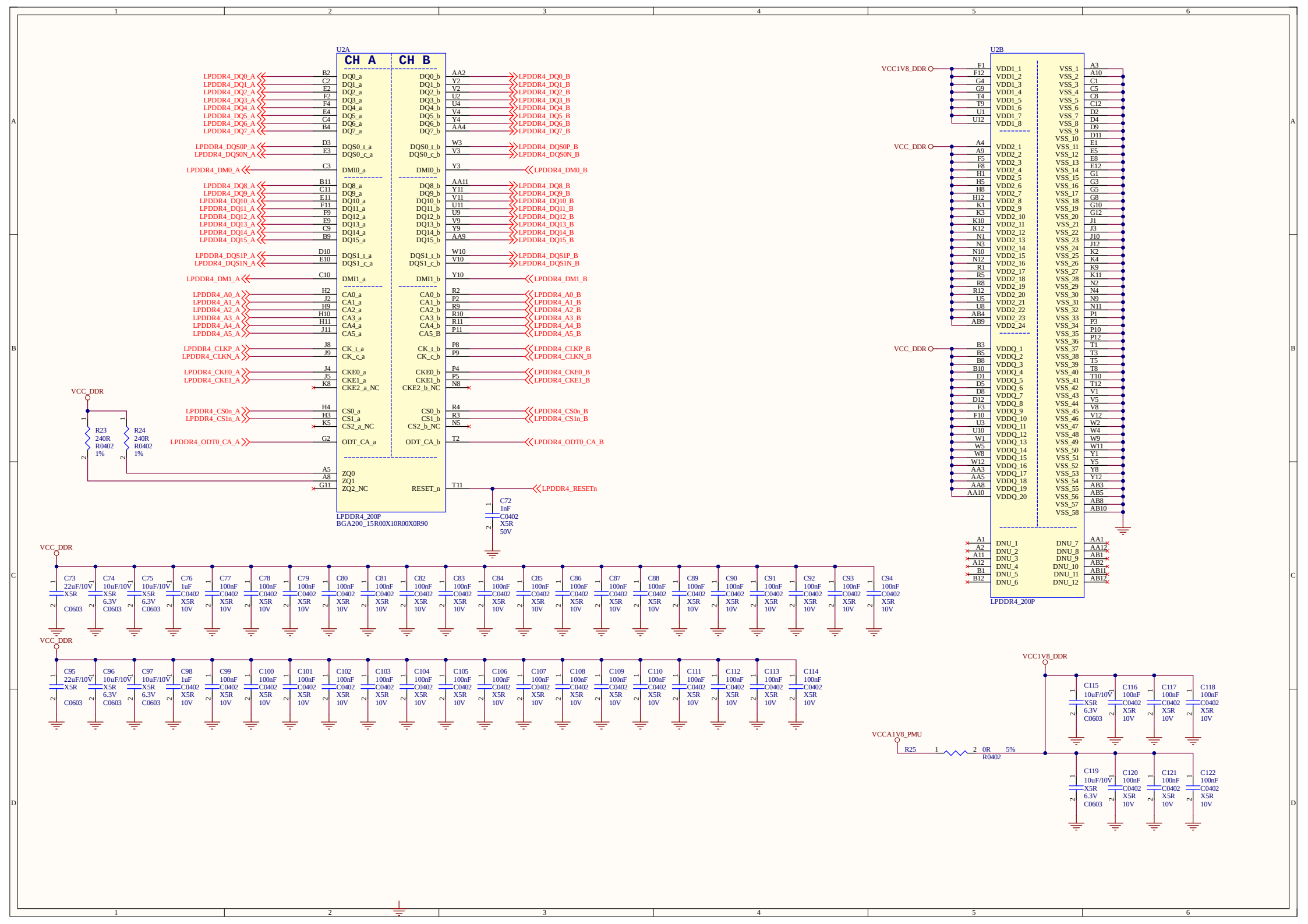
Note:

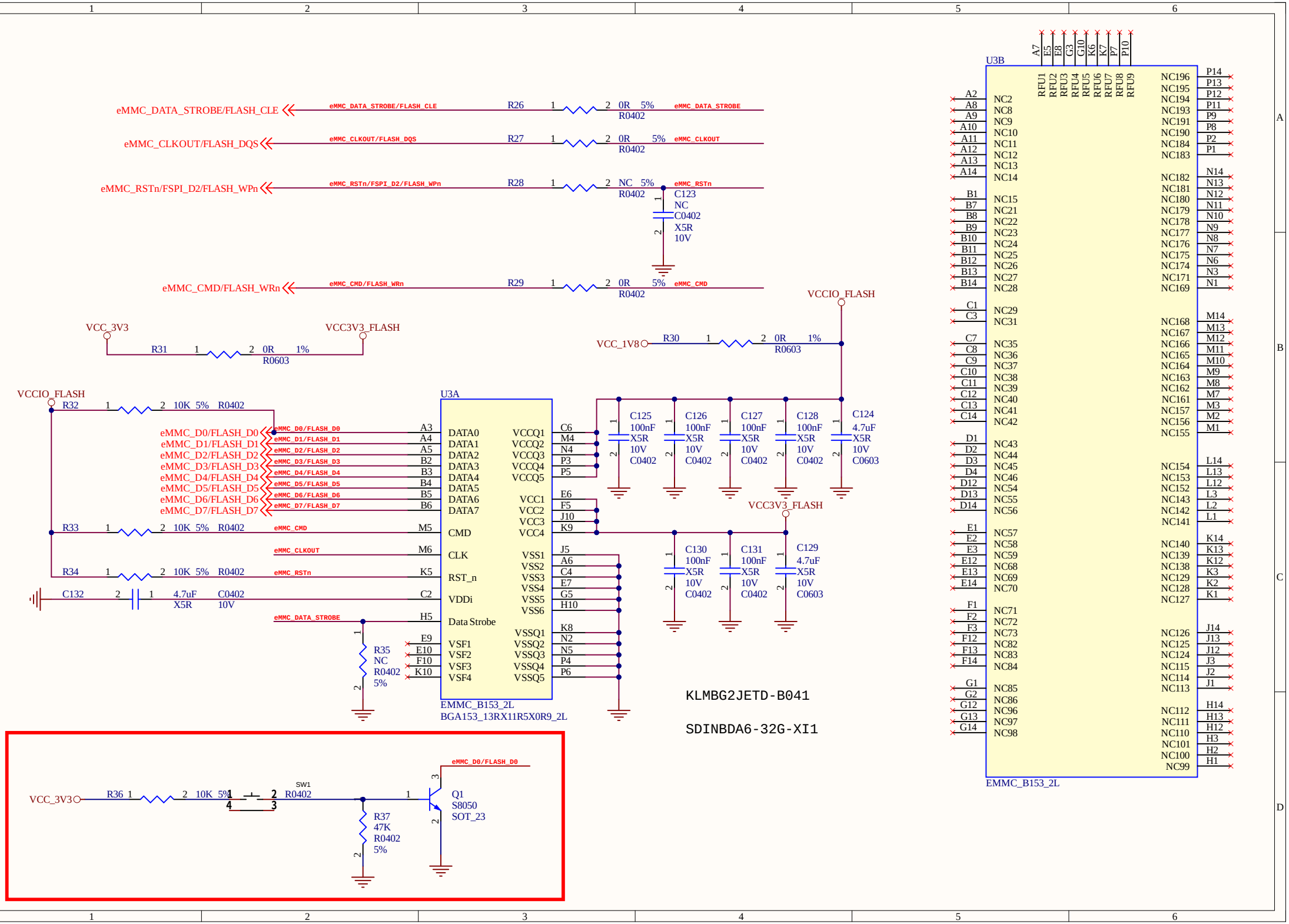
Caps of between dashed green lines and U1000 should be placed under the U1000 package

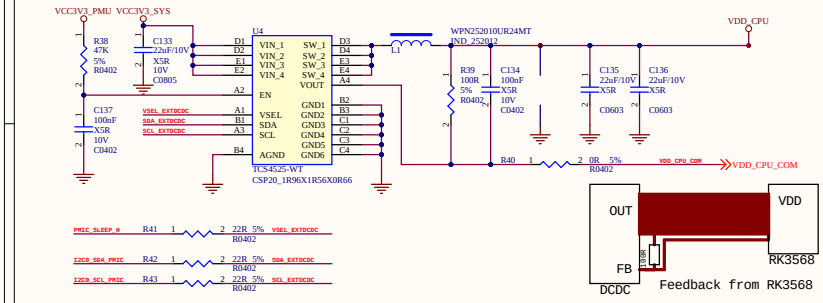
RK3568_H(VCCIO1 Domain)



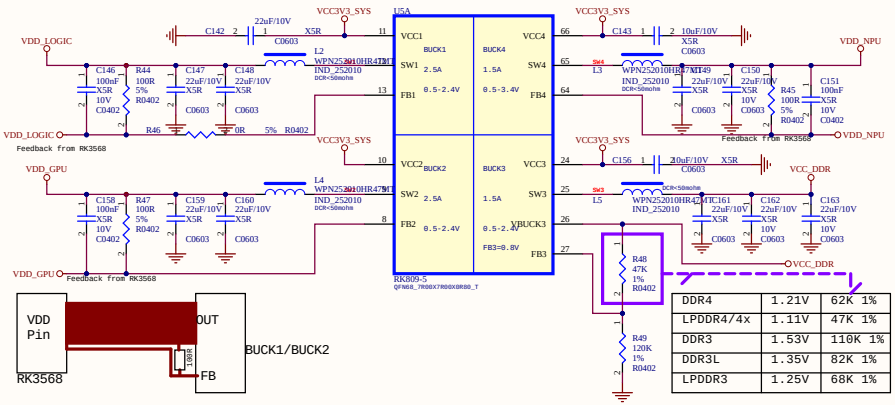
Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package


U2A
CH A
CH B
LPDDR4_DQ0_A
LPDDR4_DQ1_A
LPDDR4_DQ2_A
LPDDR4_DQ3_A
LPDDR4_DQ4_A
LPDDR4_DQ5_A
LPDDR4_DQ6_A
LPDDR4_DQ7_A
LPDDR4_DQS0P_A
LPDDR4_DQS0N_A
LPDDR4_DM0_A
LPDDR4_DQ8_A
LPDDR4_DQ9_A
LPDDR4_DQ10_A
LPDDR4_DQ11_A
LPDDR4_DQ12_A
LPDDR4_DQ13_A
LPDDR4_DQ14_A
LPDDR4_DQ15_A
LPDDR4_DQS1P_A
LPDDR4_DQS1N_A
LPDDR4_DM1_A
LPDDR4_A0_A
LPDDR4_A1_A
LPDDR4_A2_A
LPDDR4_A3_A
LPDDR4_A4_A
LPDDR4_A5_A
LPDDR4_CLKP_A
LPDDR4_CLKN_A
LPDDR4_CKE0_A
LPDDR4_CKE1_A
LPDDR4_CS0n_A
LPDDR4_CS1n_A
LPDDR4_ODT0_CA_A
LPDDR4_RESETn
LPDDR4_DQ0_B
LPDDR4_DQ1_B
LPDDR4_DQ2_B
LPDDR4_DQ3_B
LPDDR4_DQ4_B
LPDDR4_DQ5_B
LPDDR4_DQ6_B
LPDDR4_DQ7_B
LPDDR4_DQS0P_B
LPDDR4_DQS0N_B
LPDDR4_DM0_B
LPDDR4_DQ8_B
LPDDR4_DQ9_B
LPDDR4_DQ10_B
LPDDR4_DQ11_B
LPDDR4_DQ12_B
LPDDR4_DQ13_B
LPDDR4_DQ14_B
LPDDR4_DQ15_B
LPDDR4_DQS1P_B
LPDDR4_DQS1N_B
LPDDR4_DM1_B
LPDDR4_A0_B
LPDDR4_A1_B
LPDDR4_A2_B
LPDDR4_A3_B
LPDDR4_A4_B
LPDDR4_A5_B
LPDDR4_CLKP_B
LPDDR4_CLKN_B
LPDDR4_CKE0_B
LPDDR4_CKE1_B
LPDDR4_CS0n_B
LPDDR4_CS1n_B
LPDDR4_ODT0_CA_B
VCC_DDR
R23 240R R0402 1%
R24 240R R0402 1%
C72 1nF C0402 X5R 50V
LPDDR4_200P
BGA200_15R00X10R00X0R90
U2B
VCC1V8_DDR
VCC_DDR
LPDDR4_200P
C73 22uF/10V X5R C0603
C74 10uF/10V X5R 6.3V C0603
C75 10uF/10V X5R 6.3V C0603
C76 1uF C0402 X5R 10V
C77 100nF C0402 X5R 10V
C78 100nF C0402 X5R 10V
C79 100nF C0402 X5R 10V
C80 100nF C0402 X5R 10V
C81 100nF C0402 X5R 10V
C82 100nF C0402 X5R 10V
C83 100nF C0402 X5R 10V
C84 100nF C0402 X5R 10V
C85 100nF C0402 X5R 10V
C86 100nF C0402 X5R 10V
C87 100nF C0402 X5R 10V
C88 100nF C0402 X5R 10V
C89 100nF C0402 X5R 10V
C90 100nF C0402 X5R 10V
C91 100nF C0402 X5R 10V
C92 100nF C0402 X5R 10V
C93 100nF C0402 X5R 10V
C94 100nF C0402 X5R 10V
C95 22uF/10V X5R C0603
C96 10uF/10V X5R 6.3V C0603
C97 10uF/10V X5R 6.3V C0603
C98 1uF C0402 X5R 10V
C99 100nF C0402 X5R 10V
C100 100nF C0402 X5R 10V
C101 100nF C0402 X5R 10V
C102 100nF C0402 X5R 10V
C103 100nF C0402 X5R 10V
C104 100nF C0402 X5R 10V
C105 100nF C0402 X5R 10V
C106 100nF C0402 X5R 10V
C107 100nF C0402 X5R 10V
C108 100nF C0402 X5R 10V
C109 100nF C0402 X5R 10V
C110 100nF C0402 X5R 10V
C111 100nF C0402 X5R 10V
C112 100nF C0402 X5R 10V
C113 100nF C0402 X5R 10V
C114 100nF C0402 X5R 10V
VCC1V8_DDR
VCCA1V8_PMU
R25 0R R0402 5%
C115 10uF/10V X5R 6.3V C0603
C116 100nF C0402 X5R 10V
C117 100nF C0402 X5R 10V
C118 100nF C0402 X5R 10V
C119 10uF/10V X5R 6.3V C0603
C120 100nF C0402 X5R 10V
C121 100nF C0402 X5R 10V
C122 100nF C0402 X5R 10V


eMMC_DATA_STROBE/FLASH_CLE
eMMC_DATA_STROBE/FLASH_CLE
R26 1 2 0R 5% eMMC_DATA_STROBE
R0402
eMMC_CLKOUT/FLASH_DQS
eMMC_CLKOUT/FLASH_DQS
R27 1 2 0R 5% eMMC_CLKOUT
R0402
eMMC_RSTn/FSPI_D2/FLASH_WPn
eMMC_RSTn/FSPI_D2/FLASH_WPn
R28 1 2 NC 5% eMMC_RSTn
R0402
C123
NC
C0402
X5R
10V
eMMC_CMD/FLASH_WRn
eMMC_CMD/FLASH_WRn
R29 1 2 0R 5% eMMC_CMD
R0402
VCC_3V3
VCC3V3_FLASH
R31 1 2 0R 1%
R0603
VCCIO_FLASH
VCC_1V8
R30 1 2 0R 1%
R0603
VCCIO_FLASH
R32 1 2 10K 5% R0402
U3A
eMMC_D0/FLASH_D0 A3 DATA0
eMMC_D1/FLASH_D1 A4 DATA1
eMMC_D2/FLASH_D2 A5 DATA2
eMMC_D3/FLASH_D3 B2 DATA3
eMMC_D4/FLASH_D4 B3 DATA4
eMMC_D5/FLASH_D5 B4 DATA5
eMMC_D6/FLASH_D6 B5 DATA6
eMMC_D7/FLASH_D7 B6 DATA7
R33 1 2 10K 5% R0402 eMMC_CMD M5 CMD
eMMC_CLKOUT M6 CLK
R34 1 2 10K 5% R0402 eMMC_RSTn K5 RST_n
C132 2 1 4.7uF X5R C0402 10V C2 VDDi
eMMC_DATA_STROBE H5 Data Strobe
R35 NC R0402 5%
E9 VSF1
E10 VSF2
F10 VSF3
K10 VSF4
C6 VCCQ1
M4 VCCQ2
N4 VCCQ3
P3 VCCQ4
P5 VCCQ5
E6 VCC1
F5 VCC2
J10 VCC3
K9 VCC4
J5 VSS1
A6 VSS2
C4 VSS3
E7 VSS4
G5 VSS5
H10 VSS6
K8 VSSQ1
N2 VSSQ2
N5 VSSQ3
P4 VSSQ4
P6 VSSQ5
EMMC_B153_2L
BGA153_13RX11R5X0R9_2L
C125 100nF X5R 10V C0402
C126 100nF X5R 10V C0402
C127 100nF X5R 10V C0402
C128 100nF X5R 10V C0402
C124 4.7uF X5R 10V C0603
VCC3V3_FLASH
C130 100nF X5R 10V C0402
C131 100nF X5R 10V C0402
C129 4.7uF X5R 10V C0603
KLMBG2JETD-B041
SDINBDA6-32G-XI1
U3B
RFU1 A7
RFU2 E5
RFU3 E8
RFU4 G3
RFU5 G10
RFU6 K6
RFU7 K7
RFU8 P7
RFU9 P10
A2 NC2
A8 NC8
A9 NC9
A10 NC10
A11 NC11
A12 NC12
A13 NC13
A14 NC14
B1 NC15
B7 NC21
B8 NC22
B9 NC23
B10 NC24
B11 NC25
B12 NC26
B13 NC27
B14 NC28
C1 NC29
C3 NC31
C7 NC35
C8 NC36
C9 NC37
C10 NC38
C11 NC39
C12 NC40
C13 NC41
C14 NC42
D1 NC43
D2 NC44
D3 NC45
D4 NC46
D12 NC54
D13 NC55
D14 NC56
E1 NC57
E2 NC58
E3 NC59
E12 NC68
E13 NC69
E14 NC70
F1 NC71
F2 NC72
F3 NC73
F12 NC82
F13 NC83
F14 NC84
G1 NC85
G2 NC86
G12 NC96
G13 NC97
G14 NC98
P14 NC196
P13 NC195
P12 NC194
P11 NC193
P9 NC191
P8 NC190
P2 NC184
P1 NC183
N14 NC182
N13 NC181
N12 NC180
N11 NC179
N10 NC178
N9 NC177
N8 NC176
N7 NC175
N6 NC174
N3 NC171
N1 NC169
M14 NC168
M13 NC167
M12 NC166
M11 NC165
M10 NC164
M9 NC163
M8 NC162
M7 NC161
M3 NC157
M2 NC156
M1 NC155
L14 NC154
L13 NC153
L12 NC152
L3 NC143
L2 NC142
L1 NC141
K14 NC140
K13 NC139
K12 NC138
K3 NC129
K2 NC128
K1 NC127
J14 NC126
J13 NC125
J12 NC124
J3 NC115
J2 NC114
J1 NC113
H14 NC112
H13 NC111
H12 NC110
H3 NC101
H2 NC100
H1 NC99
EMMC_B153_2L
VCC_3V3
R36 1 2 10K 5%
SW1
R0402
eMMC_D0/FLASH_D0
Q1
S8050
SOT_23
R37
47K
R0402
5%

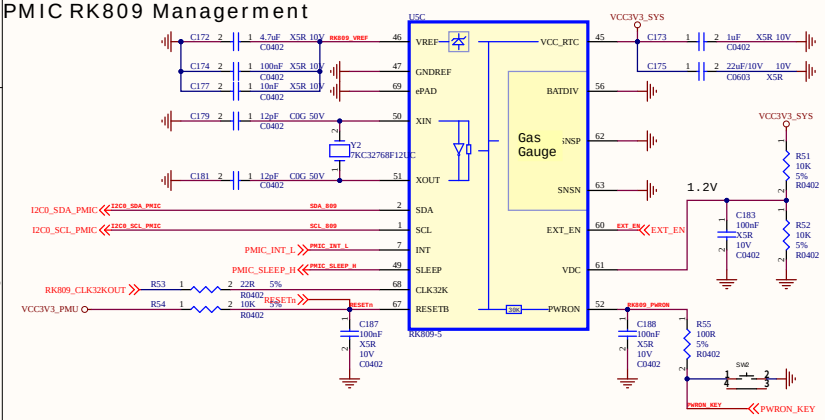


PMIC RK809 DCDC

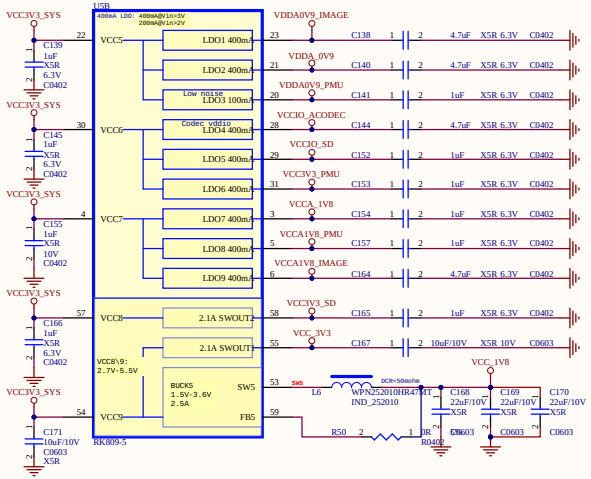


DDR4	1.21V	62K 1%
LPDDR4/4x	1.11V	47K 1%
DDR3	1.53V	110K 1%
DDR3L	1.35V	82K 1%
LPDDR3	1.25V	68K 1%

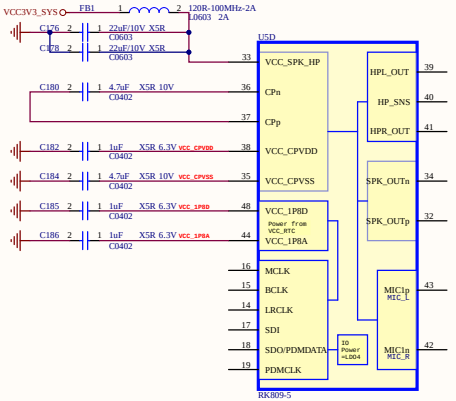
PMIC RK809 Managerment

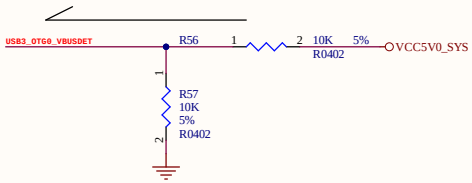


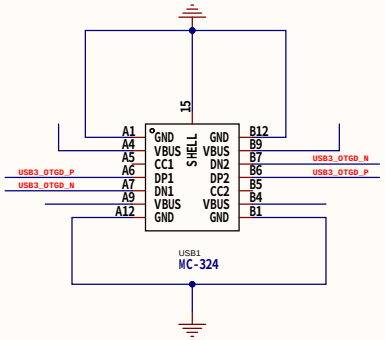
PMIC RK809 LDO

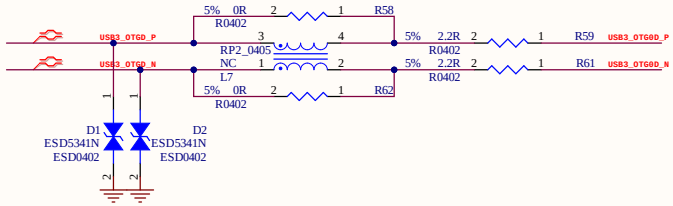


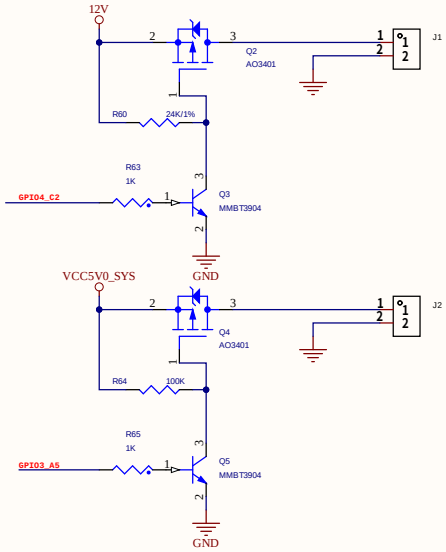
PMIC RK809 CODEC

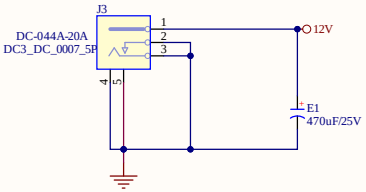




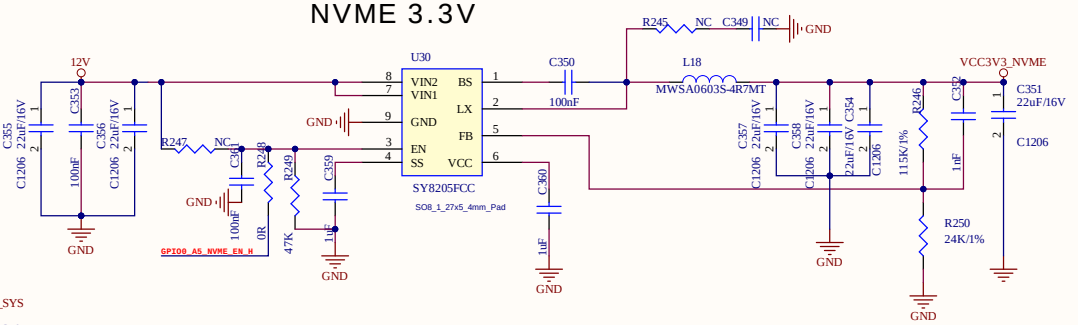






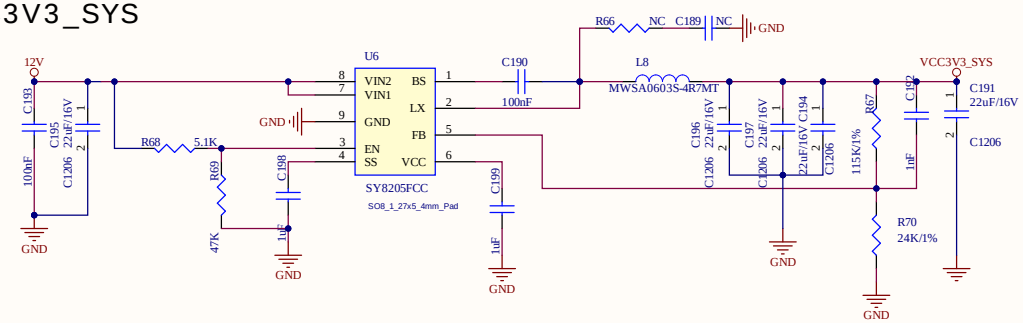


NVME 3.3V



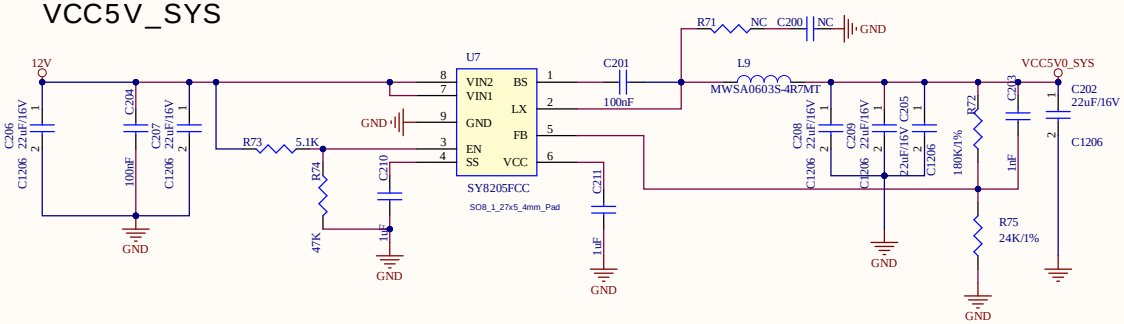
VFB=0.6V F=500KHz Imax=5A

VCC3V3_SYS

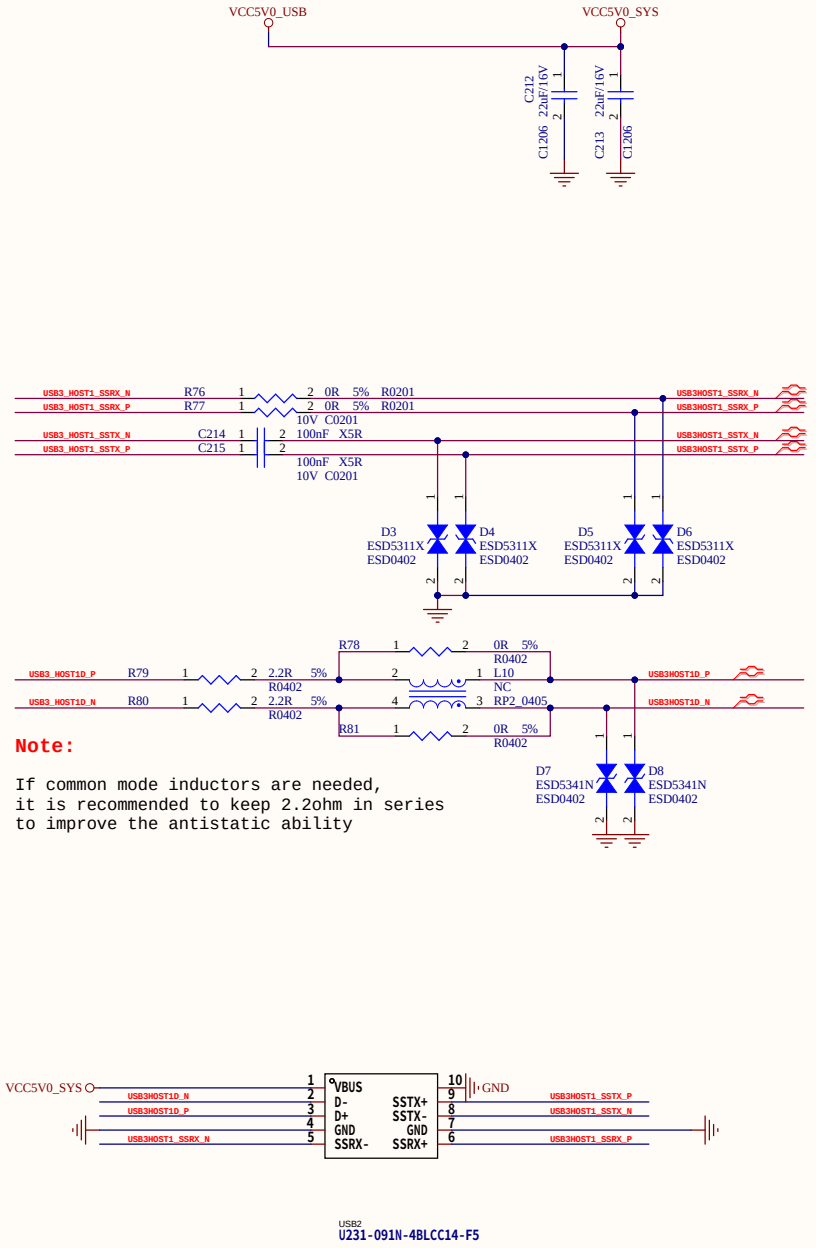


VFB=0.6V F=500KHz Imax=5A

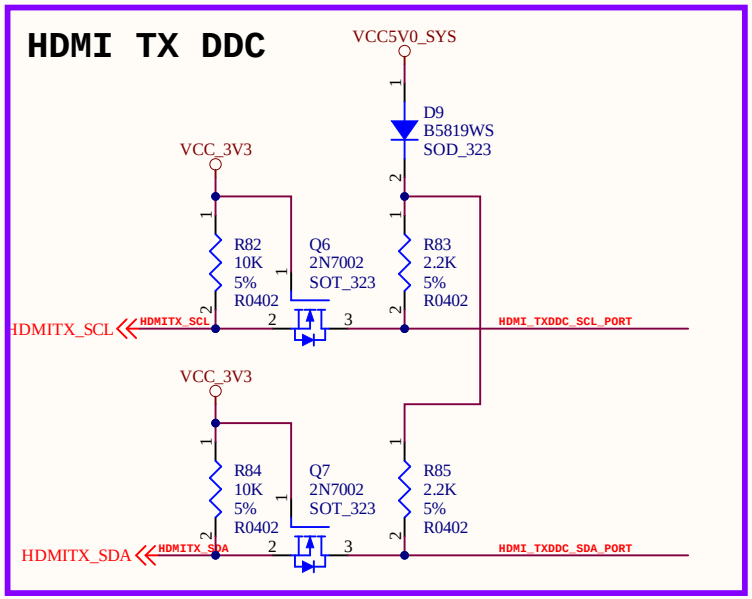
VCC5V_SYS

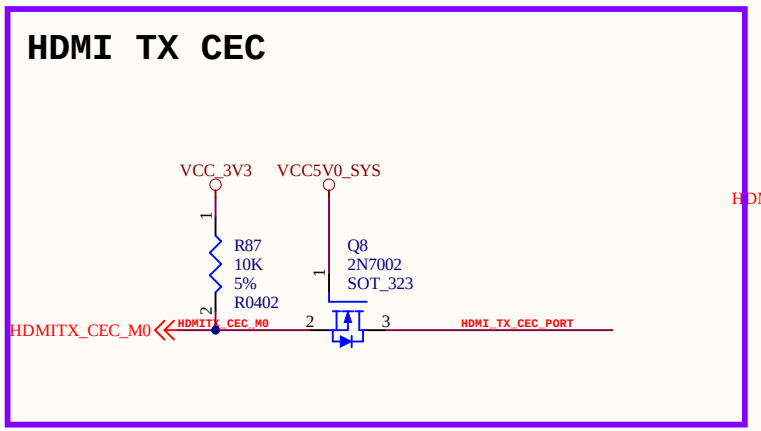


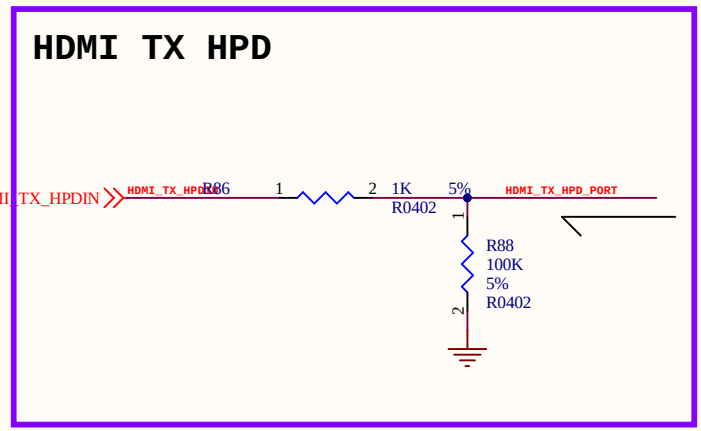
VFB=0.6V F=500KHz Imax=5A

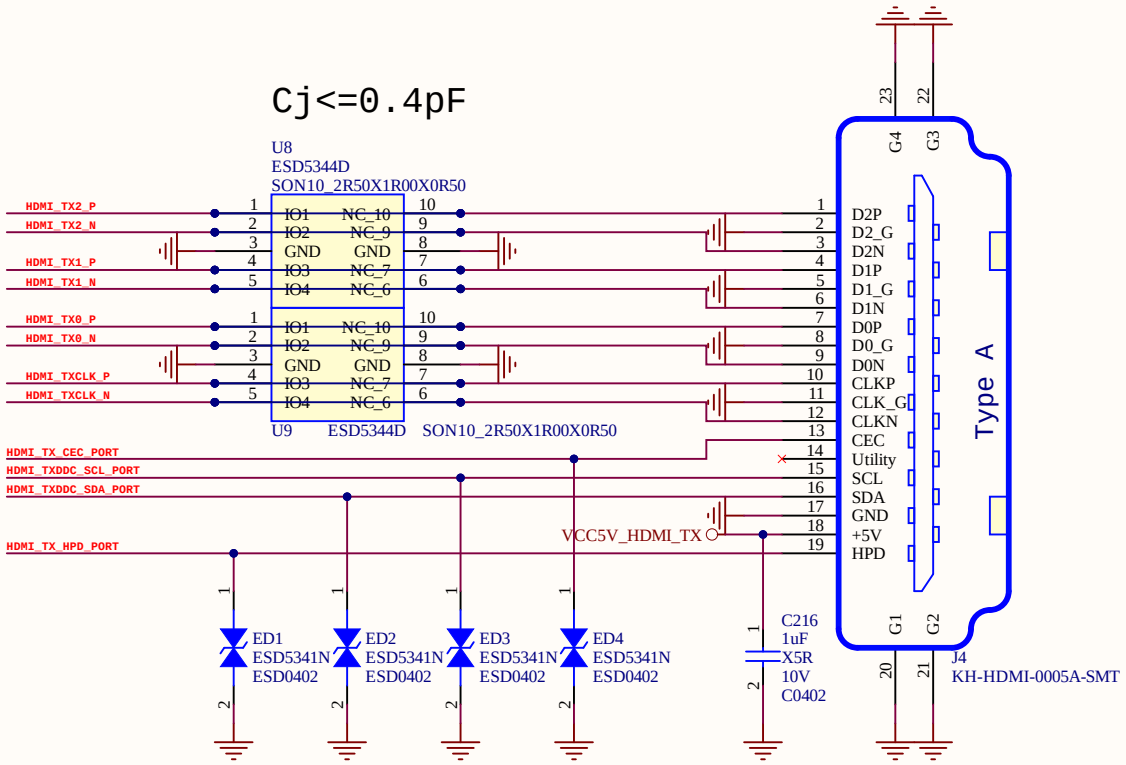

VCC5V0_USB
VCC5V0_SYS
C212 22uF/16V C1206
C213 22uF/16V C1206
USB3_HOST1_SSRX_N
USB3_HOST1_SSRX_P
USB3_HOST1_SSTX_N
USB3_HOST1_SSTX_P
R76 0R 5% R0201
R77 0R 5% R0201
10V C0201
C214 100nF X5R
C215 100nF X5R
10V C0201
USB3HOST1_SSRX_N
USB3HOST1_SSRX_P
USB3HOST1_SSTX_N
USB3HOST1_SSTX_P
D3 ESD5311X ESD0402
D4 ESD5311X ESD0402
D5 ESD5311X ESD0402
D6 ESD5311X ESD0402
USB3_HOST1D_P
USB3_HOST1D_N
R79 2.2R 5% R0402
R80 2.2R 5% R0402
R78 0R 5% R0402
L10 NC
RP2_0405
R81 0R 5% R0402
USB3HOST1D_P
USB3HOST1D_N
D7 ESD5341N ESD0402
D8 ESD5341N ESD0402
Note:
If common mode inductors are needed,
it is recommended to keep 2.2ohm in series
to improve the antistatic ability
VCC5V0_SYS
USB3HOST1D_N
USB3HOST1D_P
USB3HOST1_SSRX_N
VBUS
D-
D+
GND
SSRX-
SSTX+
SSTX-
GND
SSRX+
GND
USB3HOST1_SSTX_P
USB3HOST1_SSTX_N
USB3HOST1_SSRX_P
USB2
U231-091N-4BLCC14-F5

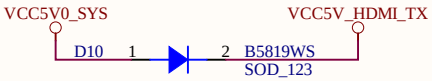
HDMI2.0 TX

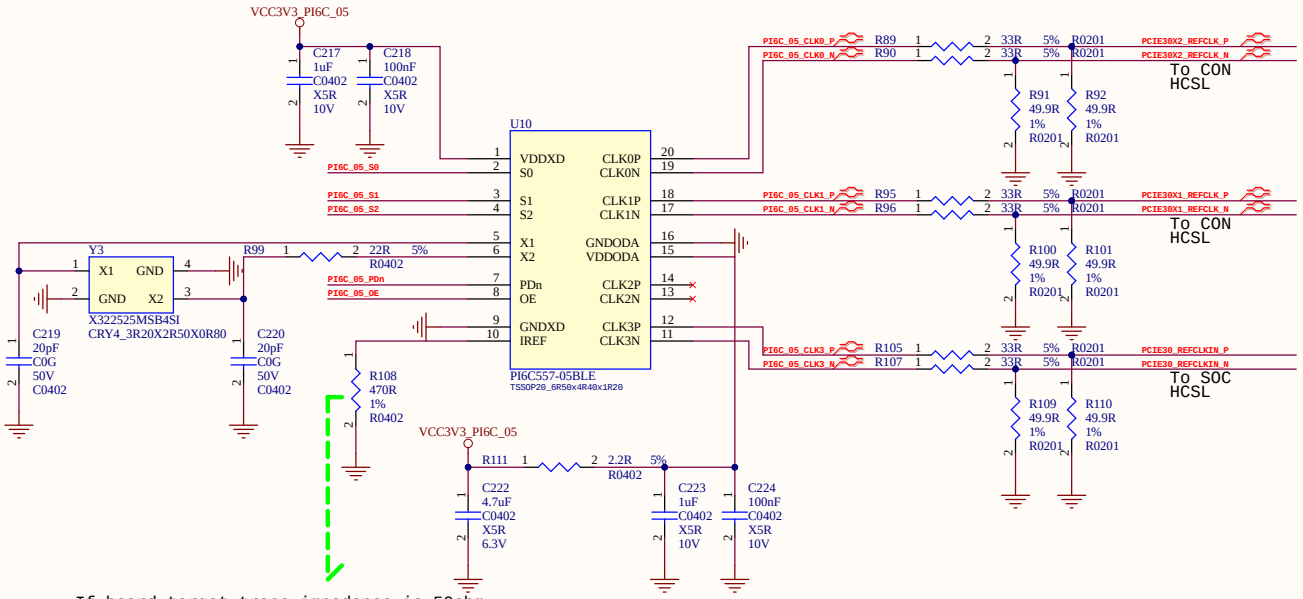

HDMI TX DDC
VCC5V0_SYS
D9
B5819WS
SOD_323
VCC_3V3
R82
10K
5%
R0402
Q6
2N7002
SOT_323
R83
2.2K
5%
R0402
HDMITX_SCL
HDMITX_SCL
HDMI_TXDDC_SCL_PORT
VCC_3V3
R84
10K
5%
R0402
Q7
2N7002
SOT_323
R85
2.2K
5%
R0402
HDMITX_SDA
HDMITX_SDA
HDMI_TXDDC_SDA_PORT


HDMI TX CEC
VCC_3V3
VCC5V0_SYS
R87
10K
5%
R0402
Q8
2N7002
SOT_323
HDMITX_CEC_M0
HDMITX_CEC_M0
HDMI_TX_CEC_PORT

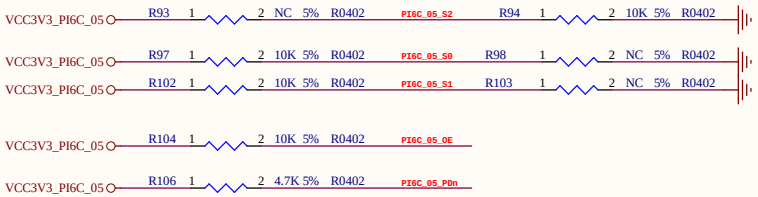

HDMI TX HPD
HDMI_TX_HPDIN
HDMI_TX_HPDIN
R86
1K
5%
R0402
HDMI_TX_HPD_PORT
R88
100K
5%
R0402

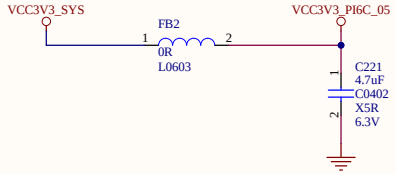

Cj<=0.4pF
U8
ESD5344D
SON10_2R50X1R00X0R50
HDMI_TX2_P
HDMI_TX2_N
HDMI_TX1_P
HDMI_TX1_N
HDMI_TX0_P
HDMI_TX0_N
HDMI_TXCLK_P
HDMI_TXCLK_N
IO1
IO2
GND
IO3
IO4
NC_10
NC_9
GND
NC_7
NC_6
U9
ESD5344D
SON10_2R50X1R00X0R50
HDMI_TX_CEC_PORT
HDMI_TXDDC_SCL_PORT
HDMI_TXDDC_SDA_PORT
HDMI_TX_HPD_PORT
VCC5V_HDMI_TX
ED1
ESD5341N
ESD0402
ED2
ESD5341N
ESD0402
ED3
ESD5341N
ESD0402
ED4
ESD5341N
ESD0402
C216
1uF
X5R
10V
C0402
D2P
D2_G
D2N
D1P
D1_G
D1N
D0P
D0_G
D0N
CLKP
CLK_G
CLKN
CEC
Utility
SCL
SDA
GND
+5V
HPD
Type A
J4
KH-HDMI-0005A-SMT


VCC5V0_SYS
D10
B5819WS
SOD_123
VCC5V_HDMI_TX



PI6C_S2	PI6C_S1	PI6C_S0	Spread %	Out Freq
0	0	0	-0.5	100MHz
0	0	1	-1.0	100MHz
0	1	0	-1.5	100MHz
0	1	1	No Spread	100MHz

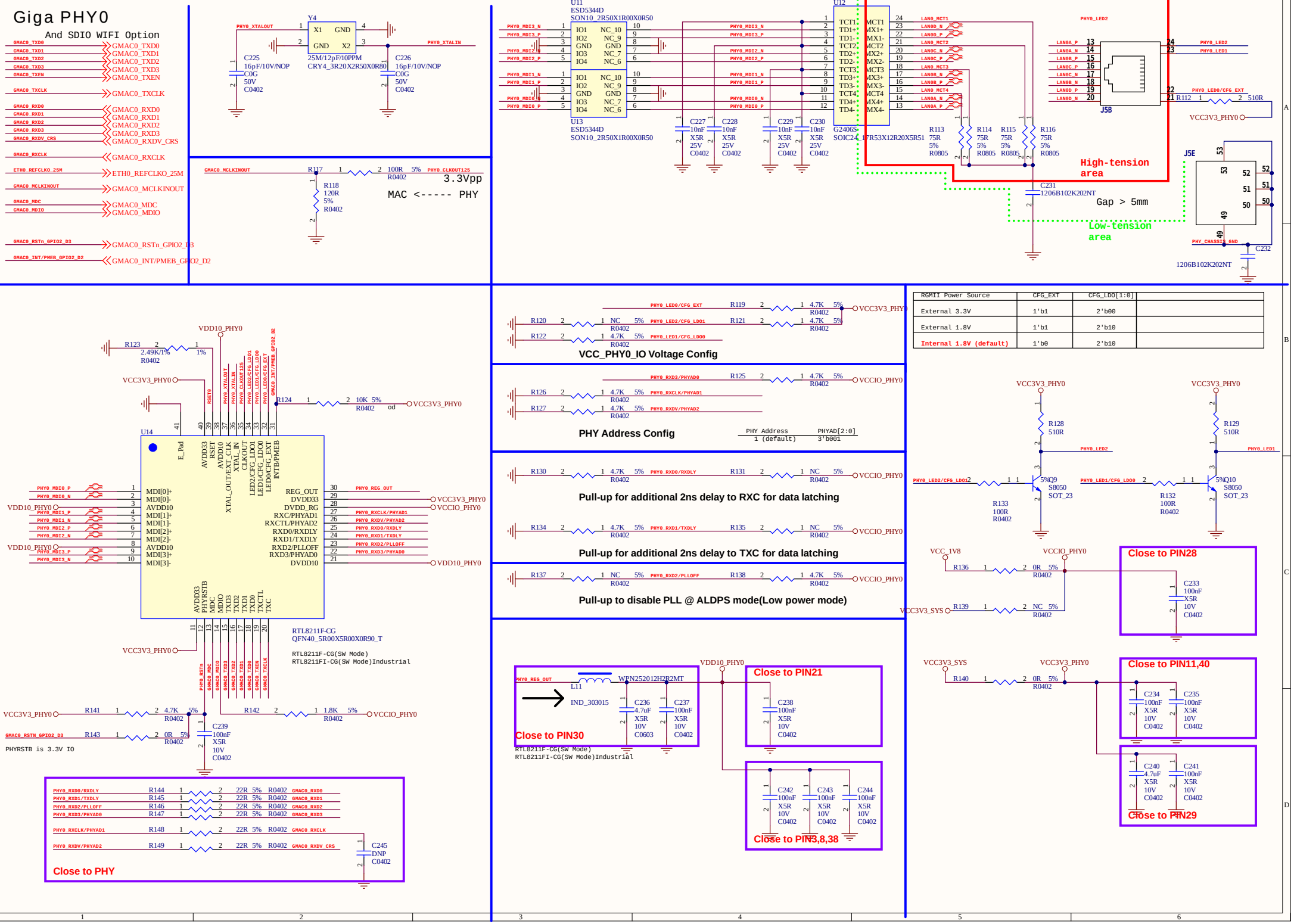




If board target trace impedance is 50ohm
then R = 475ohm providing an IREF of 2.32 mA . The output current (IOH) is 6 * IREF .
6x2.32X50=696mV

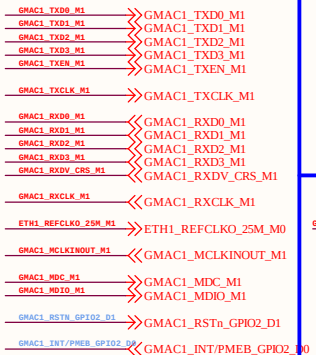
Giga PHY0

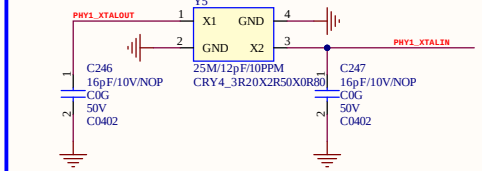
And SDIO WIFI Option

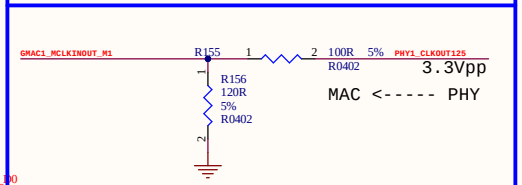


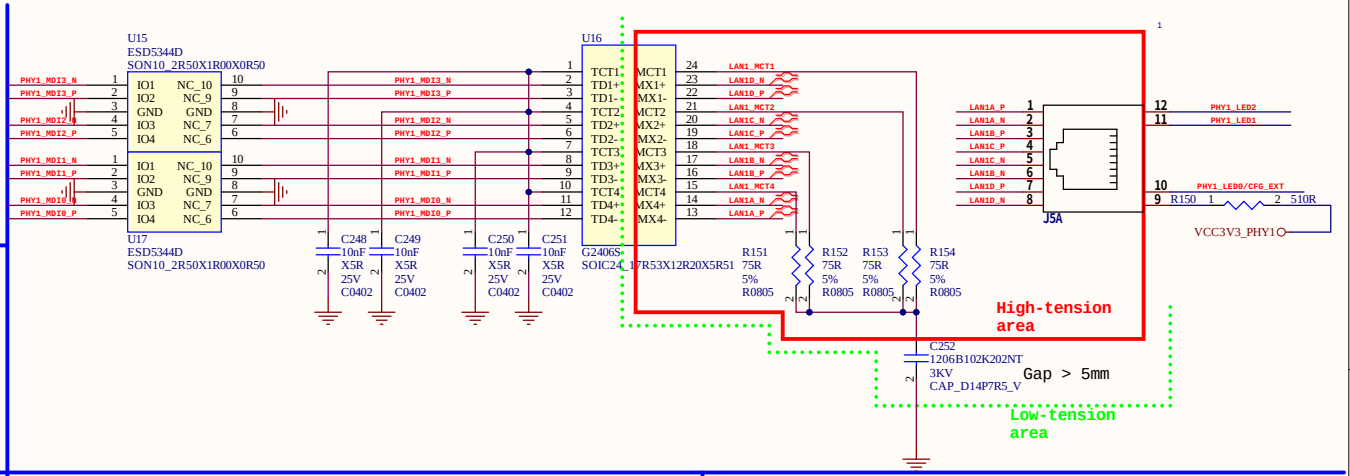
RGMII Power Source	CFG_EXT	CFG_LDO[1:0]	
External 3.3V	1'b1	2'b00	
External 1.8V	1'b1	2'b10	
Internal 1.8V (default)	1'b0	2'b10	

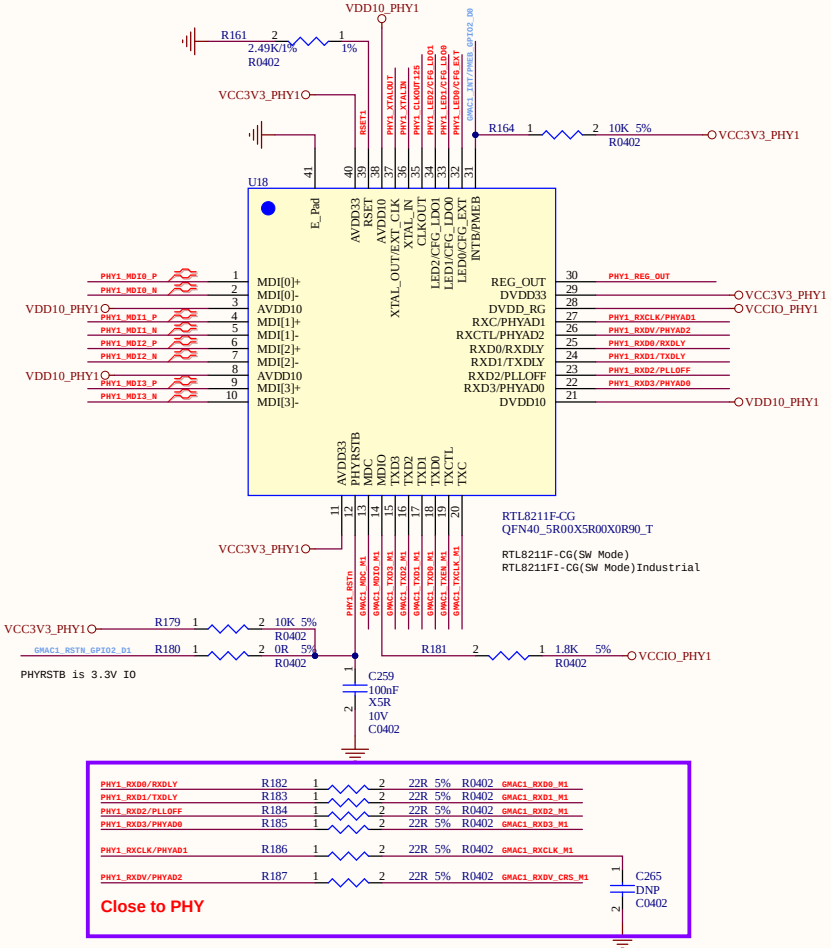
Giga PHY1

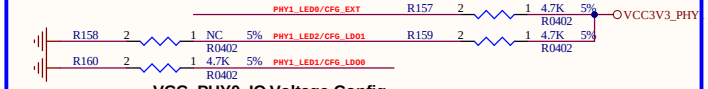


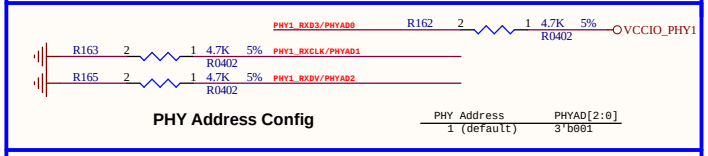


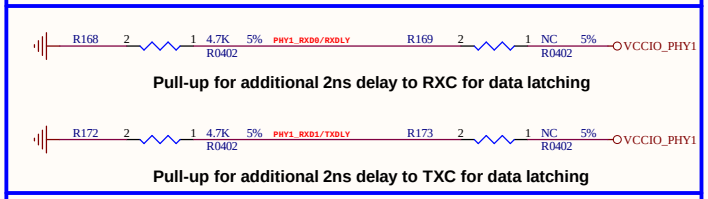


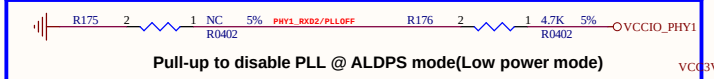


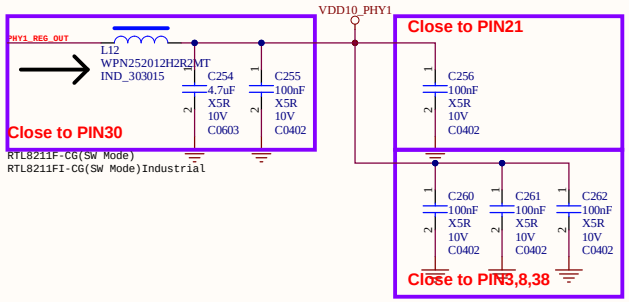




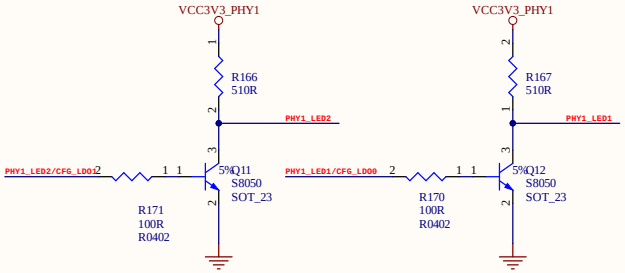


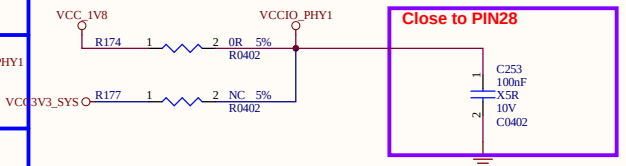


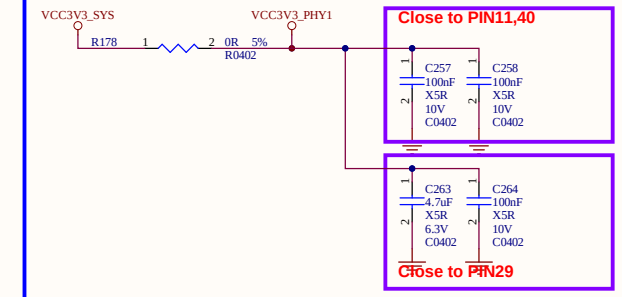


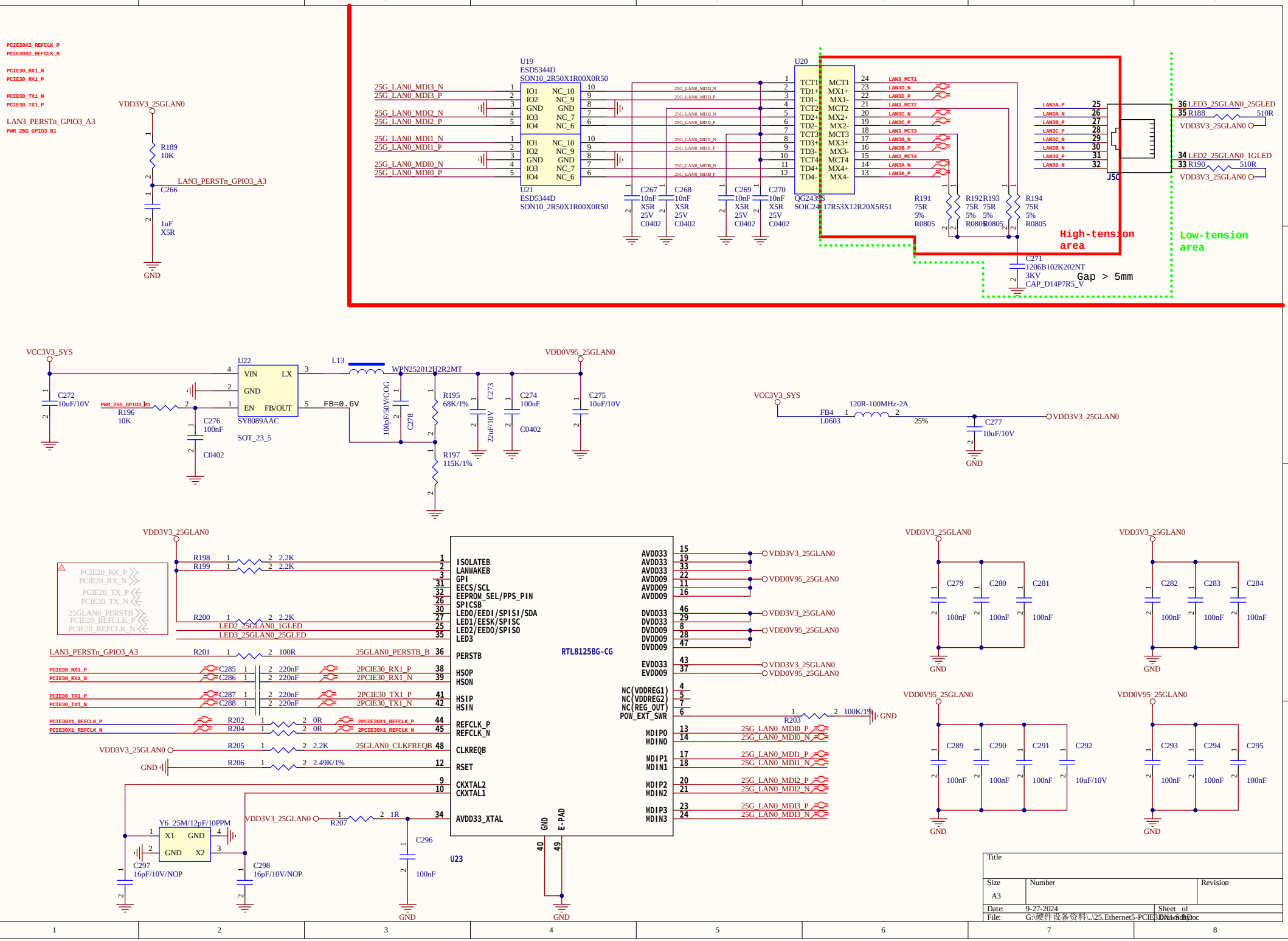


RGMII Power Source	CFG_EXT	CFG_LDO[1:0]	
External 3.3V	1'b1	2'b00	
External 1.8V	1'b1	2'b10	
Internal 1.8V(default)	1'b0	2'b10	








PCIE30X2_REFCLK_P
PCIE30X2_REFCLK_N
PCIE30_RX1_N
PCIE30_RX1_P
PCIE30_TX1_N
PCIE30_TX1_P
LAN3_PERSTn_GPIO3_A3
PWR_25G_GPIO3_B1
VDD3V3_25GLAN0
R189
10K
LAN3_PERSTn_GPIO3_A3
C266
1uF
X5R
GND
U19
ESD5344D
SON10_2R50X1R00X0R50
U21
ESD5344D
SON10_2R50X1R00X0R50
25G_LAN0_MDI3_N
25G_LAN0_MDI3_P
25G_LAN0_MDI2_N
25G_LAN0_MDI2_P
25G_LAN0_MDI1_N
25G_LAN0_MDI1_P
25G_LAN0_MDI0_N
25G_LAN0_MDI0_P
C267
C268
C269
C270
10nF
X5R
25V
C0402
U20
QG2435
SOIC24_17R53X12R20X5R51
LAN3_MCT1
LAN3D_N
LAN3D_P
LAN3_MCT2
LAN3C_N
LAN3C_P
LAN3_MCT3
LAN3B_N
LAN3B_P
LAN3_MCT4
LAN3A_N
LAN3A_P
R191
R192
R193
R194
75R
5%
R0805
J5C
LED3_25GLAN0_25GLED
R188
510R
LED2_25GLAN0_1GLED
R190
C271
1206B102K202NT
3KV
CAP_D14P7R5_V
Gap > 5mm
High-tension area
Low-tension area
VCC3V3_SYS
U22
VIN
LX
GND
EN
FB/OUT
SY8089AAC
SOT_23_5
L13
WPN252012H2R2MT
VDD0V95_25GLAN0
C272
10uF/10V
R196
10K
C276
100nF
C0402
FB=0.6V
100pF/50V/COG
C278
R195
68K/1%
R197
115K/1%
C273
22uF/10V
C274
100nF
C275
10uF/10V
VCC3V3_SYS
FB4
L0603
120R-100MHz-2A
25%
C277
10uF/10V
VDD3V3_25GLAN0
GND
PCIE20_RX_P
PCIE20_RX_N
PCIE20_TX_P
PCIE20_TX_N
25GLAN0_PERSTB
PCIE20_REFCLK_P
PCIE20_REFCLK_N
R198
R199
R200
2.2K
LED2_25GLAN0_1GLED
LED3_25GLAN0_25GLED
LAN3_PERSTn_GPIO3_A3
R201
100R
25GLAN0_PERSTB_B
C285
C286
C287
C288
220nF
2PCIE30_RX1_P
2PCIE30_RX1_N
2PCIE30_TX1_P
2PCIE30_TX1_N
R202
R204
0R
2PCIE30X1_REFCLK_P
2PCIE30X1_REFCLK_N
R205
25GLAN0_CLKFREQB
R206
2.49K/1%
Y6 25M/12pF/10PPM
X1
X2
C297
16pF/10V/NOP
C298
16pF/10V/NOP
R207
1R
C296
100nF
ISOLATEB
LANWAKEB
GPI
EECS/SCL
EEPROM_SEL/PPS_PIN
SPICSB
LED0/EEDI/SPISI/SDA
LED1/EESK/SPISC
LED2/EEDO/SPISO
LED3
PERSTB
HSOP
HSON
HSIP
HSIN
REFCLK_P
REFCLK_N
CLKREQB
RSET
CKXTAL2
CKXTAL1
AVDD33_XTAL
RTL8125BG-CG
U23
GND
E-PAD
AVDD33
DVDD33
DVDD09
EVDD33
EVDD09
NC(VDDREG1)
NC(VDDREG2)
NC(REG_OUT)
POW_EXT_SWR
R203
100K/1%
MDIP0
MDIN0
MDIP1
MDIN1
MDIP2
MDIN2
MDIP3
MDIN3
C279
C280
C281
C282
C283
C284
C289
C290
C291
C292
C293
C294
C295
100nF
10uF/10V
Title
Size
A3
Number
Revision
Date:
9-27-2024
Sheet of
File:
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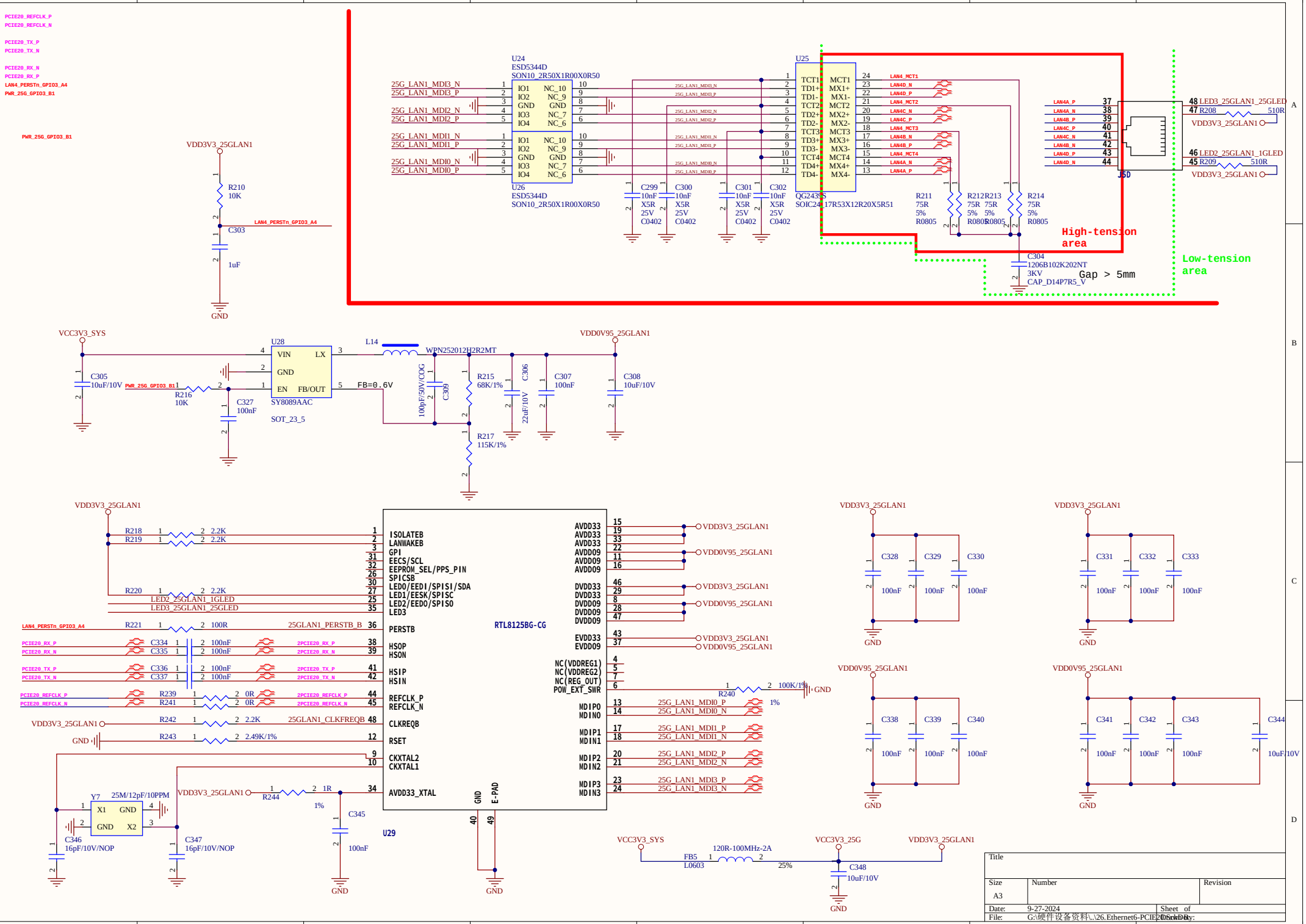
PCIE20_REFCLK_P
PCIE20_REFCLK_N
PCIE20_TX_P
PCIE20_TX_N
PCIE20_RX_N
PCIE20_RX_P
LAN4_PERSTn_GPIO3_A4
PWR_2SG_GPIO3_B1
VDD3V3_25GLAN1
R210 10K
C303 1uF
GND
U24 ESD5344D SON10_2R50X1R00X0R50
U26 ESD5344D SON10_2R50X1R00X0R50
25G_LAN1_MDI3_N
25G_LAN1_MDI3_P
25G_LAN1_MDI2_N
25G_LAN1_MDI2_P
25G_LAN1_MDI1_N
25G_LAN1_MDI1_P
25G_LAN1_MDI0_N
25G_LAN1_MDI0_P
C299 10nF X5R 25V C0402
C300 10nF X5R 25V C0402
C301 10nF X5R 25V C0402
C302 10nF X5R 25V C0402
U25
QG2435 SOIC24_17R53X12R20X5R51
LAN4_MCT1
LAN4D_N
LAN4D_P
LAN4_MCT2
LAN4C_N
LAN4C_P
LAN4_MCT3
LAN4B_N
LAN4B_P
LAN4_MCT4
LAN4A_N
LAN4A_P
R211 75R 5% R0805
R212 75R 5% R0805
R213 75R 5% R0805
R214 75R 5% R0805
J50
48 LED3_25GLAN1_25GLED
47 R208 510R
VDD3V3_25GLAN1
46 LED2_25GLAN1_1GLED
45 R209 510R
VDD3V3_25GLAN1
C304 1206B102K202NT 3KV CAP_D14P7R5_V
High-tension area
Low-tension area
Gap > 5mm
VCC3V3_SYS
U28 SY8089AAC SOT_23_5
VIN LX GND EN FB/OUT
C305 10uF/10V
R216 10K
C327 100nF
L14 WPN252012H2R2MT
FB=0.6V
100pF/50V/COG C309
R215 68K/1%
R217 115K/1%
C306 22uF/10V
C307 100nF
C308 10uF/10V
VDD0V95_25GLAN1
RTL8125BG-CG
ISOLATEB
LANWAKEB
GPI
EECS/SCL
EEPROM_SEL/PPS_PIN
SPICSB
LED0/EEDI/SPISI/SDA
LED1/EESK/SPISC
LED2/EEDO/SPISO
LED3
PERSTB
HSOP
HSON
HSIP
HSIN
REFCLK_P
REFCLK_N
CLKREQB
RSET
CKXTAL2
CKXTAL1
AVDD33_XTAL
AVDD33
DVDD33
DVDD09
EVDD33
EVDD09
NC(VDDREG1)
NC(VDDREG2)
NC(REG_OUT)
POW_EXT_SWR
MDIP0 MDIN0
MDIP1 MDIN1
MDIP2 MDIN2
MDIP3 MDIN3
E-PAD
R218 2.2K
R219 2.2K
R220 2.2K
LED2_25GLAN1_1GLED
LED3_25GLAN1_25GLED
R221 100R
25GLAN1_PERSTB_B
C334 100nF
C335 100nF
C336 100nF
C337 100nF
R239 0R
R241 0R
R242 2.2K
25GLAN1_CLKFREQB
R243 2.49K/1%
R240 100K/1%
Y7 25M/12pF/10PPM
C346 16pF/10V/NOP
C347 16pF/10V/NOP
R244 1R 1%
C345 100nF
U29
VCC3V3_SYS
FB5 L0603 120R-100MHz-2A
C348 10uF/10V
VCC3V3_25G
C328 C329 C330 C331 C332 C333 C338 C339 C340 C341 C342 C343 C344
100nF
10uF/10V
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Size A3
Number
Revision
Date: 9-27-2024
Sheet of
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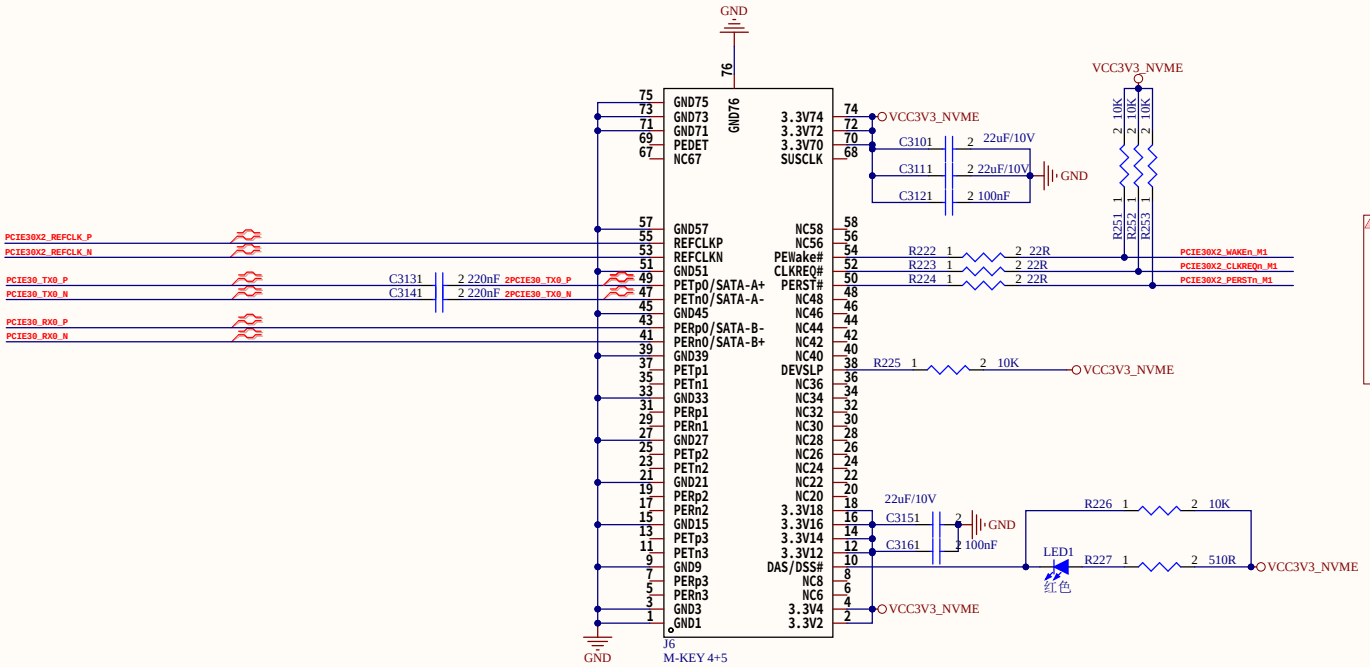
Drawn By:

PCIE30_RX0_P
PCIE30_RX0_N

PCIE30_TX0_P
PCIE30_TX0_N

PCIE30X2_REFCLK_P
PCIE30X2_REFCLK_N
PCIE20_WAKEn_M1
PCIE20_CLKREQn_M1
PCIE20_PERSTn_M1_GPIO3_C1

PCIE20_REFCLK_P
PCIE20_REFCLK_N
PCIE20_TX_P
PCIE20_TX_N
PCIE20_RX_P
PCIE20_RX_N



PCIE20_WAKEn_M1
PCIE20_CLKREQn_M1
PCIE20_PERSTn_M1

PCIE20_WAKEn_M1
PCIE20_CLKREQn_M1
PCIE20_PERSTn_M1_GPIO3_C1

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Size A3	Number	Revision
Date: 9-27-2024		Sheet of
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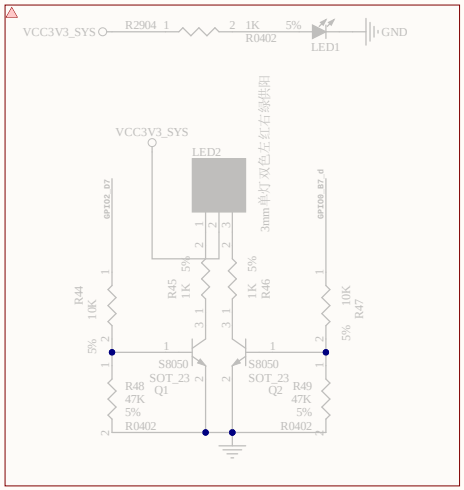
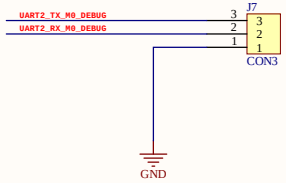
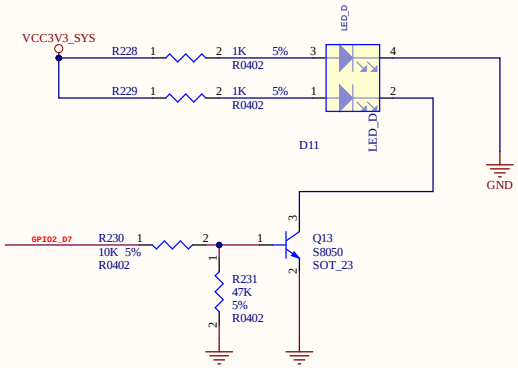
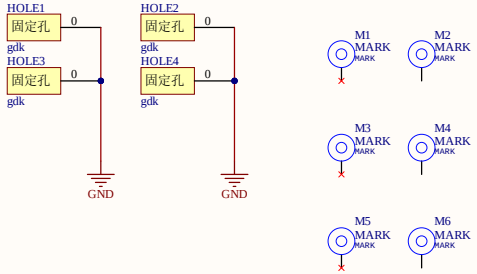
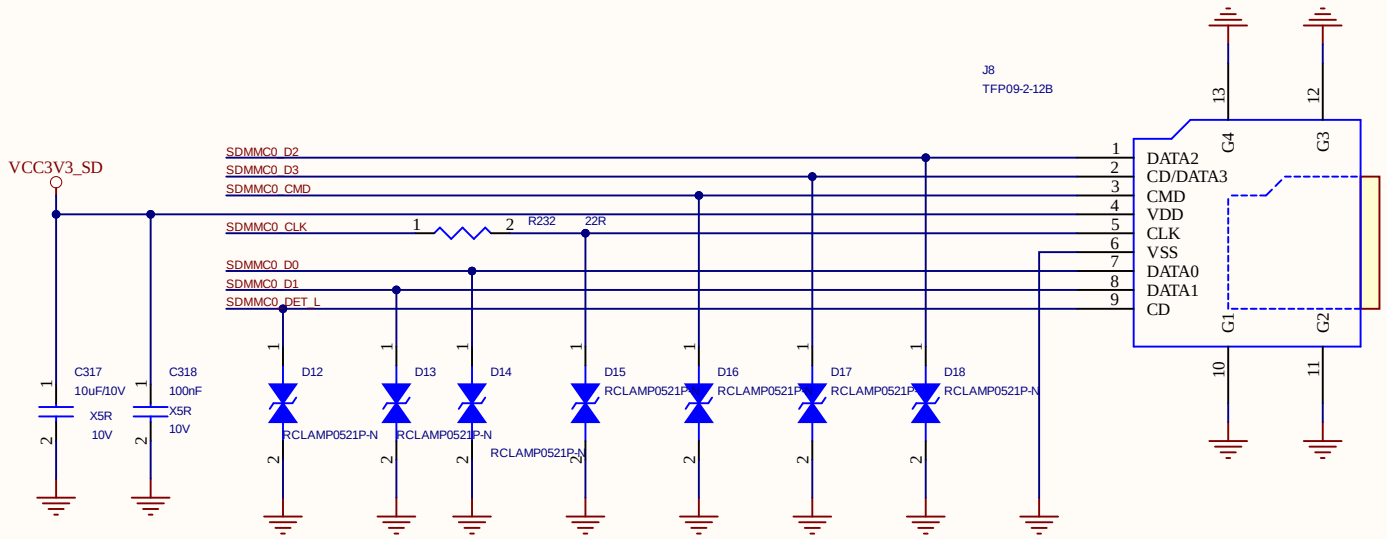
UART5_RX_M0
UART5_TX_M0
UART6_TX_M1
UART6_RX_M1
UART4_TX_M0
UART4_RX_M0



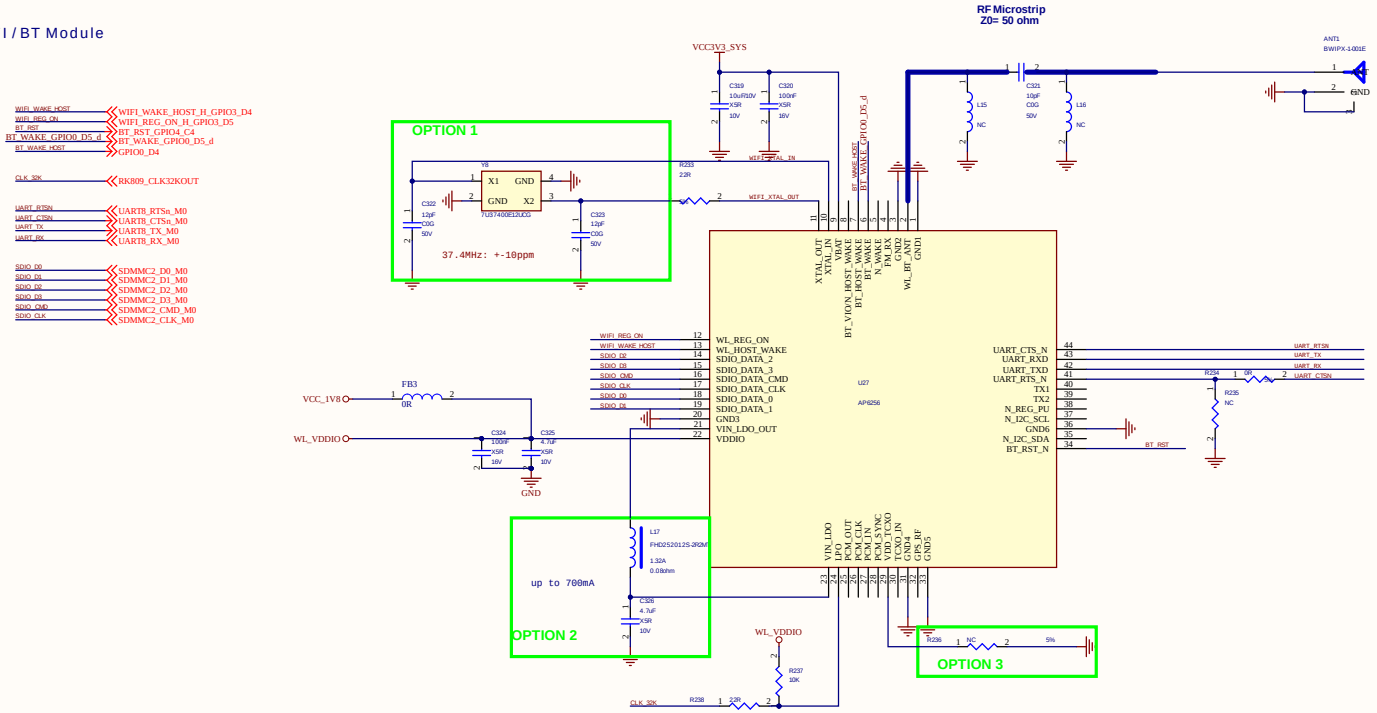







VCC3V3_SD
SDMMC0_D2
SDMMC0_D3
SDMMC0_CMD
SDMMC0_CLK
SDMMC0_D0
SDMMC0_D1
SDMMC0_DET_L
R232
22R
C317
10uF/10V
X5R
10V
C318
100nF
X5R
10V
D12
D13
D14
D15
D16
D17
D18
RCLAMP0521P-N
J8
TFP09-2-12B
DATA2
CD/DATA3
CMD
VDD
CLK
VSS
DATA0
DATA1
CD
G1
G2
G3
G4

WIFI / BT Module



OPTION	WIFI				BT	Crystals	VCCIO_SDIO	OPTION1	OPTION2	OPTION3
	a	b/g/n	ac	5GHz						
AW-CM256SM	Yes	Yes	Yes	Yes	4.2	37.4MHz	1.71-3.63V	Yes	Yes	Yes@SDIO2.0 No@SDIO3.0
AP6236/AP6212	No	Yes	No	No	4.2/4.0	26MHz	1.71-3.63V	Yes	Yes	No
AP6256/AP6255	Yes	Yes	Yes	Yes	5.0/4.2	37.4MHz	1.62-3.63V	Yes	Yes	Yes@SDIO2.0 No@SDIO3.0

Title			
Size	Number		Revision
A2			
Date:	9-27-2024	Sheet of	
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